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The design of a tape deck controller

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Department:

THE DESIGN

OF A

TAPE DECK CONTROLLER

BY

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A

THESIS

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ABSTRACT

A controller was built to interface the SCC-650 general purpose digital computer and the Kennedy Model 1400R incremental write/continuous read tape unit. All logic design information, signal lists, and tape deck instructions are included.

ACKNOWLEDGMENT

The author wishes to express his sincere appreciation to his major professor, Dr. James Tracey, for his guidence in the preparation of this thesis.

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I. INTRODUCTION

The University of Missouri at Rolla computer laboratory presently has an SCC-650 general purpose computer with a 4,096 word, 12 bit per word memory. A Teletype Model ASR-33 input/output writer, containing a keyboard input and paper tape reader capable of transferring data into the computer at a rate of ten characters (six bits) per second and a printer and paper tape punch capable of outputing information at the same rate, was supplied with the computer. This paper-tape input-output unit is extremely slow in comparision with the computer's two microsecond cycle time, requiring in excess of 20 minutes to read in some of the larger programs. The small size of the computer memory also places severe constraints on such programs as the Fortran Compiler which must be loaded in and executed in parts. A faster I/O device is clearly needed to more fully utilize this computer.

A Kennedy incremental write/continuous read tape unit was selected as a compromise between speed and monetary considerations. The advantages of incremental magnetic recording over paper tape information handling are substantial. Not only are speeds much higher (the 4,096 word memory can be filled in ten seconds and dumped onto tape in 30 seconds) and reliability greater but costs, considering necessary conversion time and hardware controller expense for other faster I/O devices, are much less.

With the purchase of this tape unit the problem of designing and building the tape deck controller remained. All instructions

necessary to the efficient use of the tape unit had to be decoded by the controller and the necessary signal sent to the tape deck. All the timing information, especially critical during data transfers, had to be monitored and controlled by this device. The complete design information for this controller as well as its operation instructions are the subjects of this thesis.

II. TAPE DECK INSTRUCTIONS

A. Continuous Read/Incremental Write Description

The Kennedy Model 1400R tape deck is a continuous read/incremental write unit. Data is presented to the recorder as levels on its six data lines. A seventh line is used to record the internally generated odd parity. Upon receiving a write command, a single character (six bits) is recorded and the tape advances one increment - 0.005 inch at 200 BPI (bits per inch). A timing pulse used in conjunction with the continuous read operation is also recorded with each piece of input data. Standard operating speed for the write operation is therefore variable within a 0-300 step per second limit and is dependent upon the rate at which the write commands are furnished. The tape deck continuous reads at 1,000 characters per second with start-stop in less than five characters. It outputs pulses on seven data lines and a clock pulse which appears for each character, regardless of content, except for all zeros. Data output therefore appears as a continuous stream of evenly spaced data words together with a clock signal.

B. Pushbutton Controls

Four momentary pushbutton controls are available on the front panel for local control of the tape deck. These buttons allow the user to place the unit in the required condition for transferring data. These functions can, however, be duplicated under remote control if the three-way Read-Write-Remote selector switch is in the Remote position.

1. Load-Forward - With the power switch on, pressing the Load-

Forward button causes the tape to be fed forward at 1,000 steps per second in search of the beginning of tape reflective strip. If the selector switch is in either the Write or the Remote position a 3.4 inch beginning of tape gap is produced immediately after the beginning of tape marker is sensed. If the switch is in the Read position, no gap is generated and the unit halts when the beginning of tape marker is sensed. If pressed at any time other than for load operation, Load-Forward causes the tape to be advanced at 1,000 steps per second as long as the button is depressed. Tape is erased as it advances if the machine is Ready.

2. Ready - Ready light indicates the tape deck is prepared to accept data. It is on at all times after the beginning of tape marker is sensed except when a Rewind command is given. It normally achieves this state automatically as described above. Pressing Ready and Load-Forward together will place the unit in the Ready condition without the presence of the beginning of tape marker if desired. This option is handy if the tape deck is powered up somewhere in the middle of the tape and it is desired to make the unit ready at that point rather than Rewind and pass over the beginning of tape marker.
3. File Gap - A standard IBM file gap with file mark is inserted when button is depressed. (See Appendix E.)
4. Rewind - Once initiated, Rewind cannot be stopped until the beginning of tape is reached. Tape will stop when the load point reflective strip is sensed. Inertia will carry the

marker several feet into the supply reel however. To remove tape the Load-Forward and Rewind pushbuttons must be pressed simultaneously until tape runs off the take-up reel.

C. Loading Instructions

1. Open dust cover by inserting middle finger in the circular indentation on the left side of the dust cover and pulling gently.
2. Place a full reel of tape containing a beginning of tape reflective strip on the supply reel hub (left). Make sure the reel is on perfectly straight before the knob in the center of the tape reel is tightened by turning it in a clockwise direction.
3. Thread tape through guide, over head and across capstan to take-up reel (see Figure 1).
4. Wind several turns manually on take-up reel (be sure not to wind the tape passed the beginning of tape reflective strip).
5. Make sure the toggle switch located below the left hub inside the dust cover is in the ON position and that the Read-Write-Remote selector switch on the front panel is in the Remote position.
6. Turn S-Pac power switch (toggle) to the ON position.
7. Power up the SCC-650 computer as follows: (a) hold the Start button down, (b) depress Power On button, (c) after five seconds, release Start button. (The Start button will

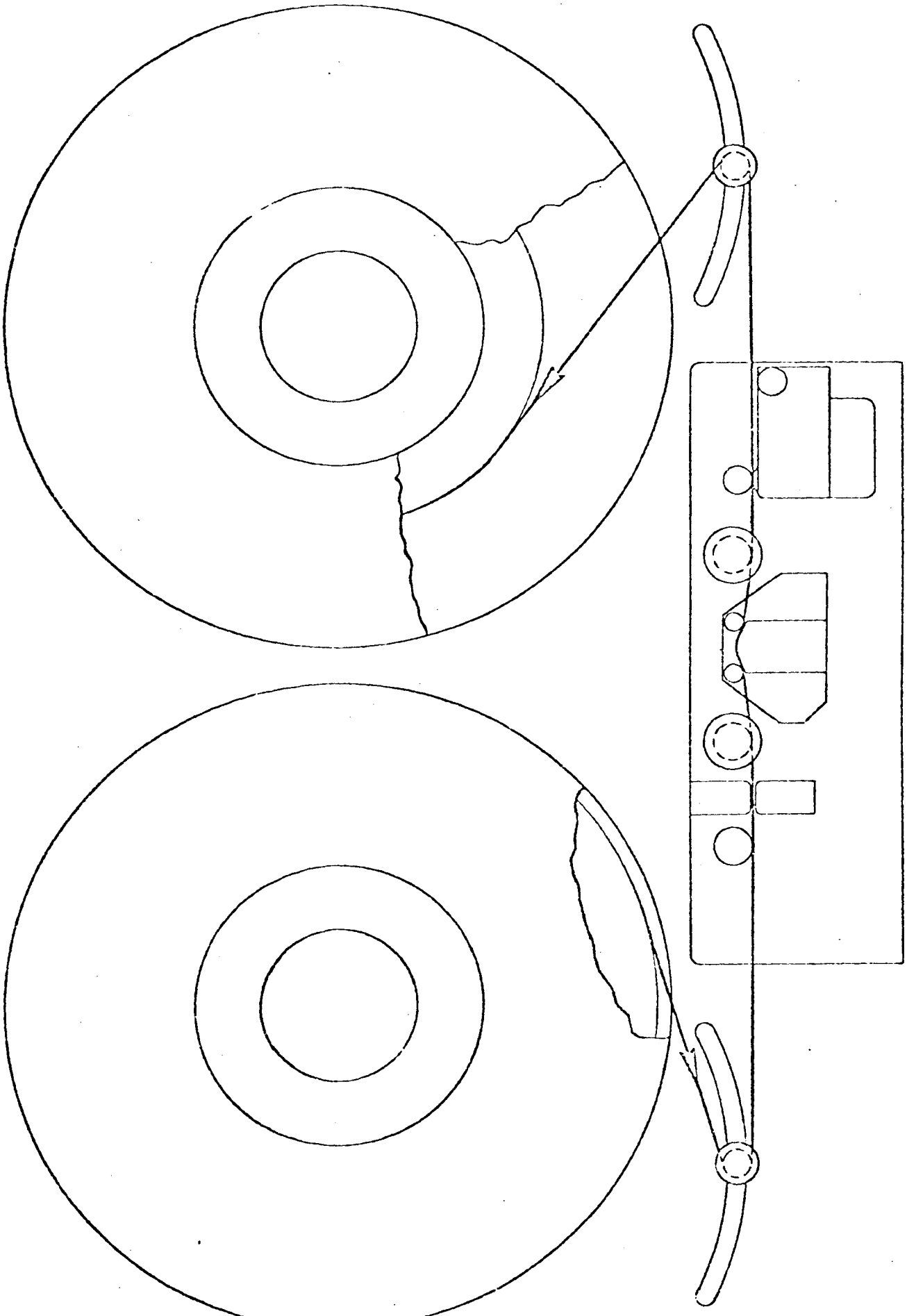

Figure 1. Tape Path

clear all registers in the S-Pac cabinet.)

8. Press Load-Forward pushbutton on tape deck and release. The machine will search for the beginning of tape marker.
9. The Ready light should now be on, indicating that the recorder is ready to receive data.

D. Input/Output Instructions

Data transfer between the SCC-650 and the Kennedy Model 1400R tape deck is accomplished exclusively over the I/O buss (the direct memory access channel is not used). A resident program in the central processing unit (CPU) is required to: (a) select the device and condition it for data transfer, (b) determine when the device is ready to transfer data, (c) monitor control functions within the device, and (d) terminate the device at completion of information transfer. The I/O instructions, which are used to accomplish this communication, have the following basic format:

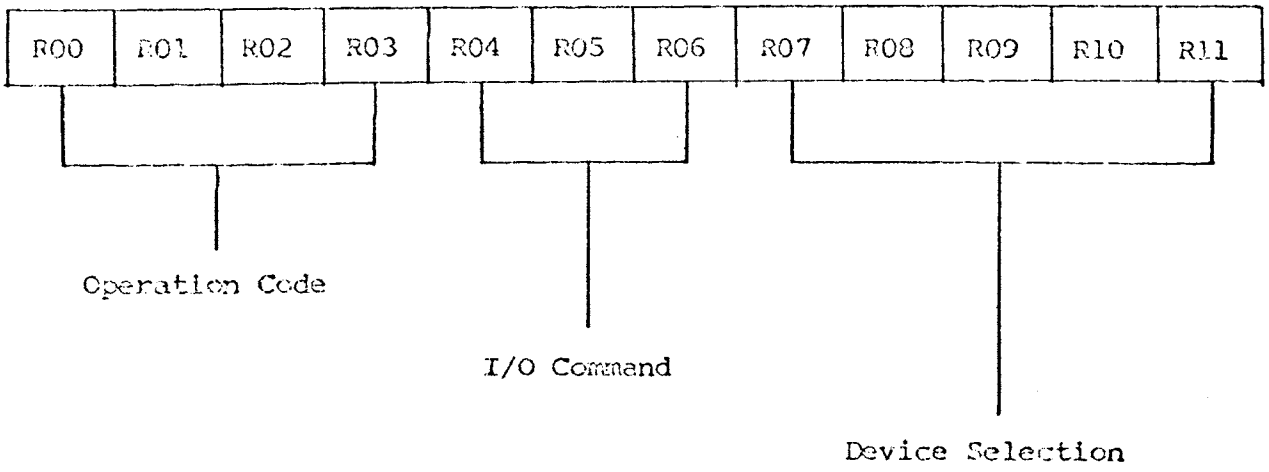

Figure 2. The R Register Format for I/O Instructions

1. Operation Code - The operation code for the I/O instructions is $(0001)_2$. This decode is available at the interface as (IOPB-).

2. I/O Command - The three signals (R04B-), (R05B-), and (R06B-) represent each bit of the I/O command. These signals are available on the I/O connector and are decoded by the external device to determine the exact I/O command. Four of the most frequently used I/O commands have been decoded by the central processor and presented at the interface as (TTAB-), (TFAB-), (DSTB-), and (SDFB-). These signals are the logic AND of IOP and four different combinations of R04 through R06. These four signals represent the Transmit to Accumulator, Transmit from Accumulator, Device Status, and Skip on Device Flag I/O commands respectively.

3. Device Selection - These five bits of the device select code are decoded by the external device to determine the device which is to respond to the I/O command. They are presented as (R07B-), (R08B-), (R09B-), (R10B-), and (R11B-) at the interface. The codes for the device selection portion of the instruction are arbitrarily assigned a pseudo octal code consisting of two bits (#7 and #8) for the first octal number and three bits (#9, #10, and #11) for the second octal number. Two device codes have been reserved for the Kennedy tape deck: (a) '14 - Magnetic Tape Read and (b) '34 - Magnetic Tape Write (where the character ' designates octal).

The basic I/O instructions can now be stated:

a.	'0714	SEL '14	Select Magnetic Tape Read
b.	'0734	SEL '34	Select Magnetic Tape Write
c.	'0654	TMR '14	Terminate Magnetic Tape Read
d.	'0674	TMR '34	Terminate Magentic Tape Write
e.	'0474	TFA '34	Transfer from Accumulator
f.	'0414	TTA '14	Transfer to Accumulator
g.	'0614	EXU '14	Execute Magnetic Tape Read
h.	'0634	EXU '34	Execute Magnetic Tape Write
i.	'0514	DST '14	Input Device Status
j.	'0534	DST '34	Input Device Status
k.	'0554	SDF '14	Skip on Device Flag

Each I/O instruction causes a number of operations to take place in the magnetic tape controller. A basic understanding of these operations can be very helpful in writing effective software. The eleven basic I/O instructions will therefore be described in more detail. For a greater insight into the operation of these instructions, the interested reader is referred to the logic diagrams.

Select Magnetic Tape Read

All flip-flops in the magnetic tape controller are cleared. The magnetic tape read select flip-flop is then set and the magnetic tape reader is electrically connected to the computer.

Select Magnetic Tape Write

All flip-flops in the magnetic tape controller are cleared.

The magnetic tape write select flip-flop is then set and the magnetic tape writer is electrically connected to the computer. The tape ready flip-flop is also set signifying that the controller is ready for the anticipated TFA command.

Terminate Magnetic Tape Read or Write

All flip-flops in the magnetic tape controller are cleared and the tape deck is electrically disconnected from the computer. (The controller, however, remains connected at the I/O buss.) This command must not be given until the final data transfer has been completed. The magnetic tape writer must not be terminated until approximately 3.5 milliseconds after the last TFA command is given. An easy way to accomplish this is simply to transfer one additional piece of data and then terminate.

Transfer from the Accumulator

If the magnetic tape writer is ready, the contents of the accumulator are transferred to the tape buffer register in the controller. The computer than executes the next sequential instruction. Since the word length in the SCC-650 is 12 bits and the magnetic tape deck has only six data channels, the controller must provide the logic necessary to give a TFA command the capability to initiate two six-bit transfers into the tape deck for each 12-bit transfer from the computer to the tape deck controller. Each six-bit transfer requires 3.33 milliseconds; therefore there is a 6.66 millisecond time lapse between the execution of two successive TFA commands. When a TFA command is executed and the device is not

ready, the computer skips the next instruction. The contents of the accumulator remain unchanged throughout this instruction. Approximately 30 seconds is required to dump 4K of memory onto tape.

Transfer to the Accumulator

When the first TTA command is given, the magnetic tape reader is not ready and so the computer skips the next instruction. This command, however, initiates two six-bit transfers from the tape deck into the tape buffer holding register in the controller. Each transfer takes one millisecond to complete; therefore two milliseconds after a TTA command is given a ready signal is transmitted to the computer. The data is then transferred into the accumulator and the computer executes the next sequential instruction. In this case, the transfer has already been completed when the TTA command is finally executed and the tape deck can be immediately terminated if desired. Approximately 10 seconds is required to fill 4K of memory.

Execute Magnetic Tape Read or Write

The magnetic tape deck is instructed to regard the contents of the accumulator as a command word. The rightmost five bits can be most conveniently loaded with the load accumulator literal command.

A00	A01	A02	A03	A04	A05	A06	A07	A08	A09	A10	A11

Figure 3. The Accumulator Format for Execute Instructions

A04 = 1 Make tape Ready.

A05 = 1 Load-Forward, find beginning of tape gap, and make the tape deck Ready.

A06 = 1 Terminate a Remote Load-Forward.

A07 = 1 Initiate a Remote Load-Forward.

A08 = 1 Operate drive stepper motor in reverse.

= 0 Operate drive stepper motor in the forward direction.

A09 = 1 Initiate a Remote Rewind.

A10 = 1 Generate a gap on the magnetic tape. The type of gap is determined by the value of bit A11.

A11 = 1 Initiate an End of Record Gap.

= 0 Initiate an End of File Gap.

Gap commands will be ignored if the tape unit is in the read status.

Input Device Status

This command is a skip test which allows the computer to test to determine if all data transfers have been completed (tape not necessarily halted). If the operation is completed, the next instruction will be executed and the status will transfer into the accumulator as follows:

A00 = 1 Tape unit is at end of reel.

A01 = 1 Tape unit is at the beginning of reel.

A02 = 1 Tape is broken.

A03 = 1 A gap is being generated.

A04 = 1 The tape unit ready light is on.

A05 = 1 A gap is being read.

A06 = 1 Tape unit file is protected.

A07 = 1 Tape unit Read-Write-Remote selector switch is in the Write position.

A08 = 1 Tape unit Read-Write-Remote selector switch is in the Read position.

A09 = 1 Tape unit Read-Write-Remote selector switch is in the Remote position.

A10 = 1 I/O error occurred during last I/O operation.

A11 = 1 Not used, always one.

Skip on Device Flag

This command is a skip test which allows the computer to test to determine if the tape has located a gap when reading. If the tape unit has located a gap, the next instruction will be executed.

NOTE:

Interrupt and I/O Error Facilities

The Echo Check Parity Output signal from the tape unit is made available at the interface on both the external interrupt (EXTINT) and the input-output error (IOE) lines. Two methods are therefore available to the programmer for error detecting while writing onto tape. At present there is no means of program disabling the external interrupt; it can, however, be disabled manually if necessary (see page 73).

III. CONCLUDING REMARKS

An effort was made in the building of the Kennedy Tape Deck controller to obtain a powerful hardware capability. An effective software package, however, is essential to obtain maximum benefit from the available hardware. An access program, written in bootstrap format and loaded from paper tape with the ability to scan the tape, locate gaps, examine header labels to find the desired program, read this program into memory starting at the programmer specified starting address, and finally terminate the tape unit after the programmer specified ending address has been filled, would be a tremendous start. All other programs could then be permanently stored on tape and conveniently and quickly accessed once this program was in memory. Even the write program, used to locate a blank piece of tape, generate a gap, write a header label, write the desired program onto tape (again specifying only the beginning and ending addresses), write an End of File Gap, and finally terminate the tape unit, could be among these permanently stored programs.

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4. Pottinger, H. (1968) A Formal Description of the SCC 650 Digital Computer. Technical Report CRL 68.1. Rolla, Missouri. 45p.

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APPENDIX A

S-Pac Information

1. Card Description

Nine different types of S-Pac cards were used in the design of the tape deck controller. The model number, descriptive name, as well as the number and type of circuits on each card is given below.

a. The NAND Type 2 Pac, model number DI-20 (200-KC card) or DI-35 (5-MC card), contains eight two-input NAND gates.

b. The Diode Pac, model number DC-20 (200-KC card) or DC-35 (5-MC card), contains one two-input NAND gate, five three-input diode clusters, and two two-input diode clusters.

c. The Parallel NAND Type 2 Pac, model number DJ-20 (200-KC card), contains six two-input NAND gates with separate load circuits.

d. The NAND Type 1 Pac, model number DN-20 (200-KC card) or DN-35 (5-MC card), contains four two-input NAND gates, two two-input diode clusters, and two three-input diode clusters.

e. The Power Amplifier Pac, model number PA-30 (1-MC card) or PA-35 (5-MC card), contains four power amplifiers.

f. The Gated Flip-Flop Pac, model number FA-35 (5-MC card), contains four flip-flops with AC input gating.

g. The Counter Pac, model number BC-35 (5-MC card), contains four flip-flops for binary counting.

h. The Basic Flip-Flop Pac, model number FF-35 (5-MC card) contains four flip-flops with DC input gating.

i. The Delay Multivibrator/Pulse Shaper Pac, model number DM-20A (200-KC card) or DM-35A (5-MC card), contains three monostable

multivibrators with adjustable pulse widths.

2. Circuit Description

These nine cards contain only seven distinctly different circuits. The logic levels for these circuits are -6 volts (logic ONE) and 0 volts (logic ZERO). A brief description of each of these circuits is given below.

a. The Diode Cluster essentially functions as an AND gate in all its applications. Hence the following symbol has been adopted.

Figure 4. Diode Cluster Symbol

b. The NAND Gate consists of a diode cluster coupled directly to a single transistor inverter amplifier. Therefore its symbol follows naturally.

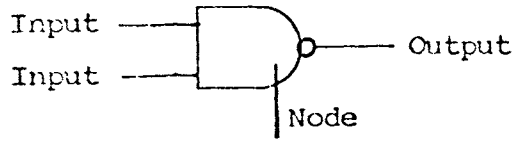


Figure 5. NAND Gate Symbol

All inputs are diode buffered and the output is either the voltage of a saturated transistor or the clamp voltage (-6 volts). When all inputs are at -6 volts or open, the transistor is turned on and the output is driven to ground through the saturated transistor. If an input is at ground, the transistor is turned off and the output falls to the

clamp voltage of -6 volts.

c. The Power Amplifier is a logic equivalent of the S-Pac NAND gate and is used to drive heavy loads, such as common reset lines. Each power amplifier has a single diode input plus node and two isolated outputs. (CAUTION: The outputs of power amplifiers cannot be shorted together to perform an OR operation.) Its logic symbol is shown below.

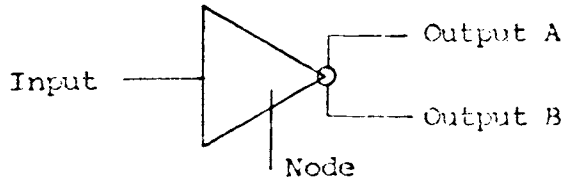


Figure 6. Power Amplifier Symbol

d. The Basic Flip-Flop circuit consists of two cross-coupled NAND gates with DC set and reset inputs and set and reset outputs. A flip-flop is considered to be in the ONE state when its SET output is a logic ONE. Setting or resetting is accomplished by applying a logic ZERO to the set or reset input respectively. A no-input signal is treated as a logic ONE. (See Figure 7.)

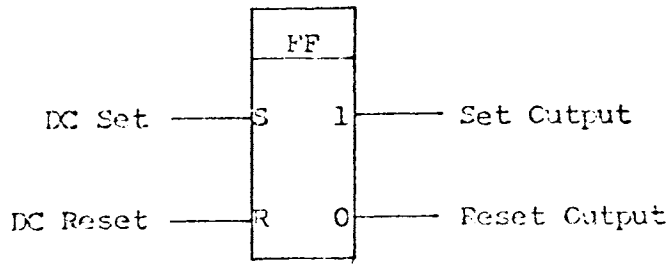


Figure 7. Basic Flip-Flop Symbol

e. The Gated Flip-Flop consists of two cross-coupled NAND gates with AC-coupled inputs. This flip-flop is set or reset each time a positive going 6-volt step is applied to the set or reset input respectively. A positive going pulse applied to the common reset input clears (resets) all four flip-flops on the card. (See Figure 8.)

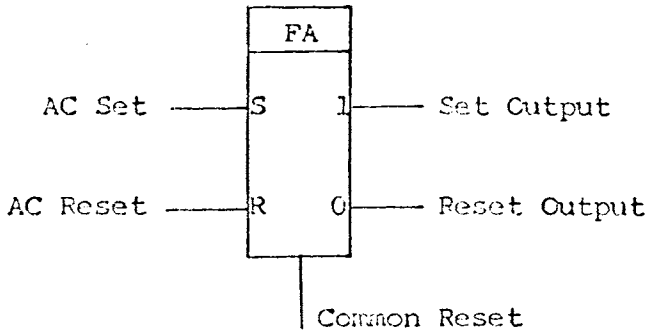


Figure 8. Gated Flip-Flop Symbol

f. The Counter Pac contains four 5-MC counter stages which can be wired for binary operations or used as independent complementing flip-flops. The AC set and reset input function exactly as the Gated Flip-Flop above. A logic ONE to logic ZERO transition on the toggle input causes the flip-flop to change state. Cascaded toggle flip-flops comprise a counter. A positive going pulse applied to the common reset input clears (resets) all four flip-flops on the card. (See Figure 9.)

g. The Delay Multivibrator (Single-Shot) has an AC trigger input

sensitive to positive going pulses. Two outputs, an assertion and a negation output (see Figure 10) are available on each circuit. Various built-in capacitors can be wired into the circuit to obtain the desired delay. Externally connected capacitors can be used to obtain longer pulse widths up to several seconds. A potentiometer in the circuit can also be used to adjust the pulse width over the range determined by the particular capacitor selected.

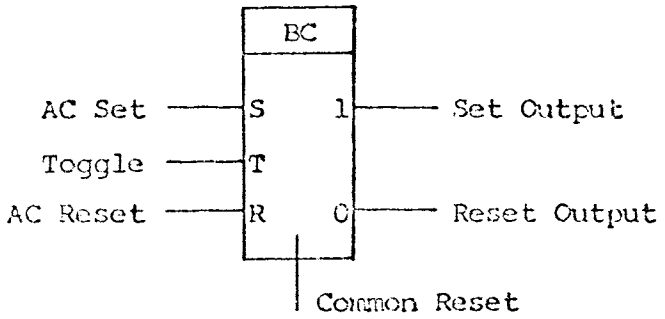


Figure 9. Counter Flip-Flop Symbol

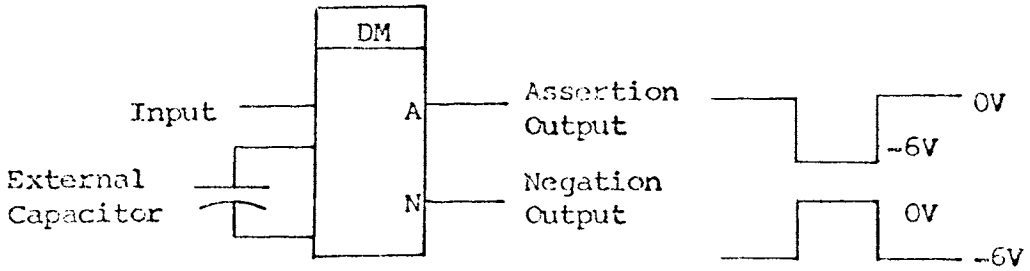


Figure 10. Delay Multivibrator Symbol

APPENDIX B

Logic Level Converters and Special Circuitry

1. Level Converters

The logic levels used in the central processing unit of the SCC-650 are: (a) 0 volts, representing logic ZERO, and (b) +8 volts, representing logic ONE. Since all the signals that are available on the I/O buss are passed through standard driver inverters, these signals appear at the connector as low true signals, that is: (a) 0 volts, representing logic ONE, and (b) +8 volts, representing logic ZERO. The logic levels in the S-Pacs (tape deck controller) are: (a) 0 volts, representing logic ZERO and (b) -6 volts, representing logic ONE. The logic levels in the tape deck are the same as the computer's, that is: (a) 0 volts, representing logic ZERO, and (b) +8 volts, representing logic ONE. Therefore the level converters that are needed between the computer, controller and tape deck are designated as follows:

a. LC1 - transfer from the computer to the controller

b. LC2 - transfer from the controller to the computer

c. LC3 - transfer from the tape deck to the controller

d. LC4 - transfer from the controller to the tape deck

The circuitry for LC1 and LC3 is exactly the same (see Figure 11). The speed up capacitor, however, is used only with the 125 nanosecond timing pulses coming from the computer.

The circuitry for LC2 and LC4 (see Figure 12 and 13) differs only in the removal of the collector resistor, diode, and 25 volt

power supply. This is done to prevent this circuit from loading down the I/O buss when the S-Pac power supply is off.

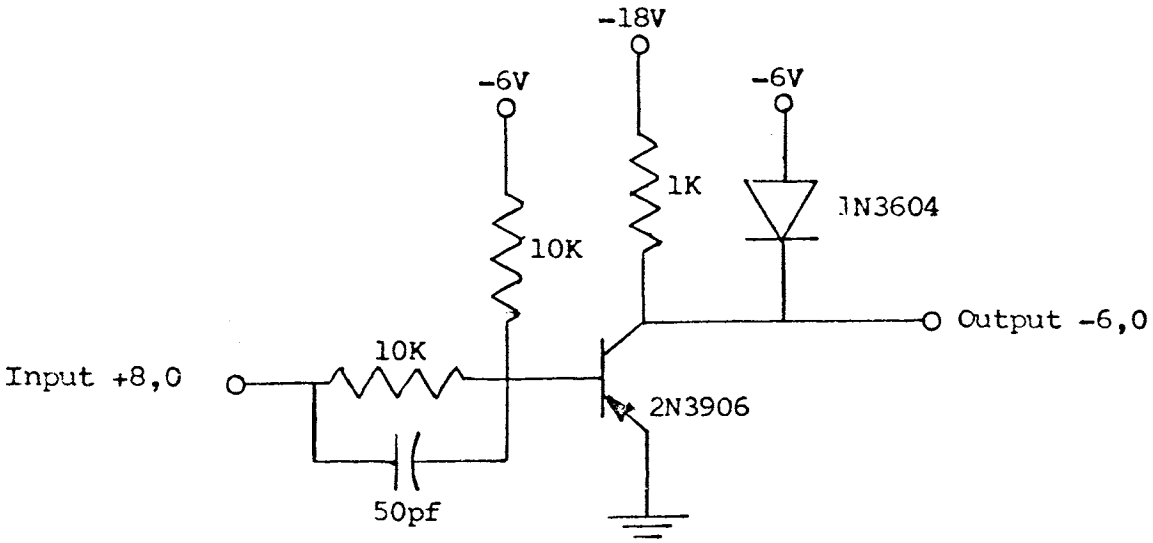


Figure 11. Logic Level Converter (+8,0 into -6,0)

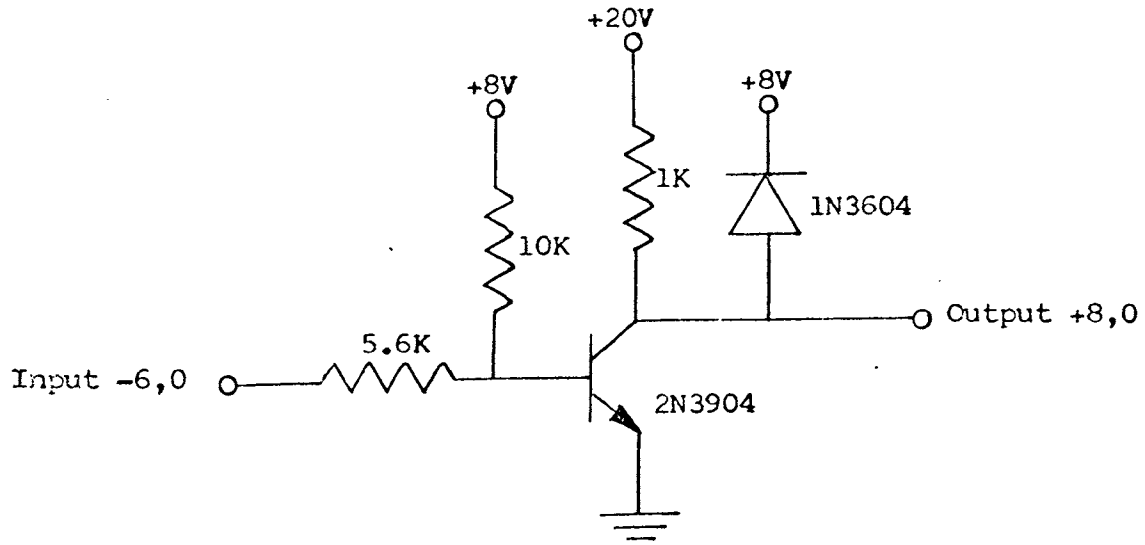


Figure 12. Logic Level Converter (-6,0 from controller into +8,0 of the tape deck)

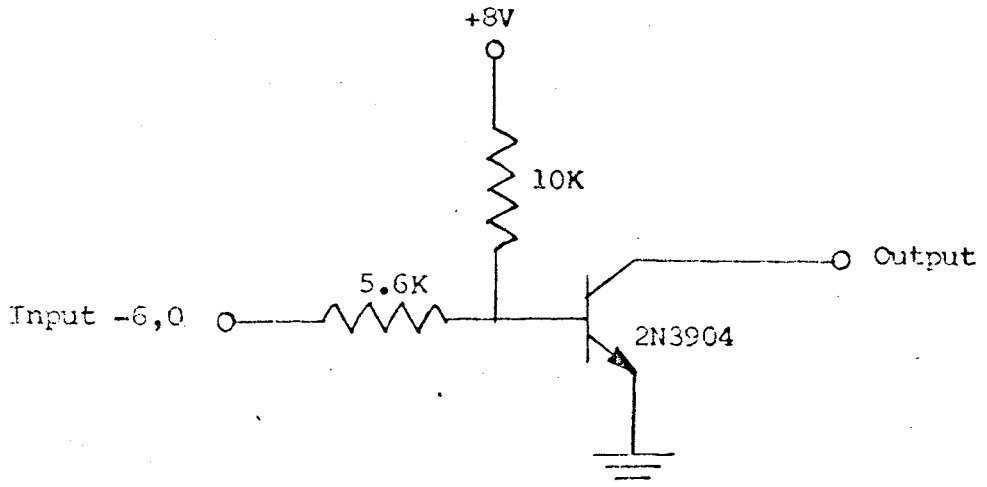


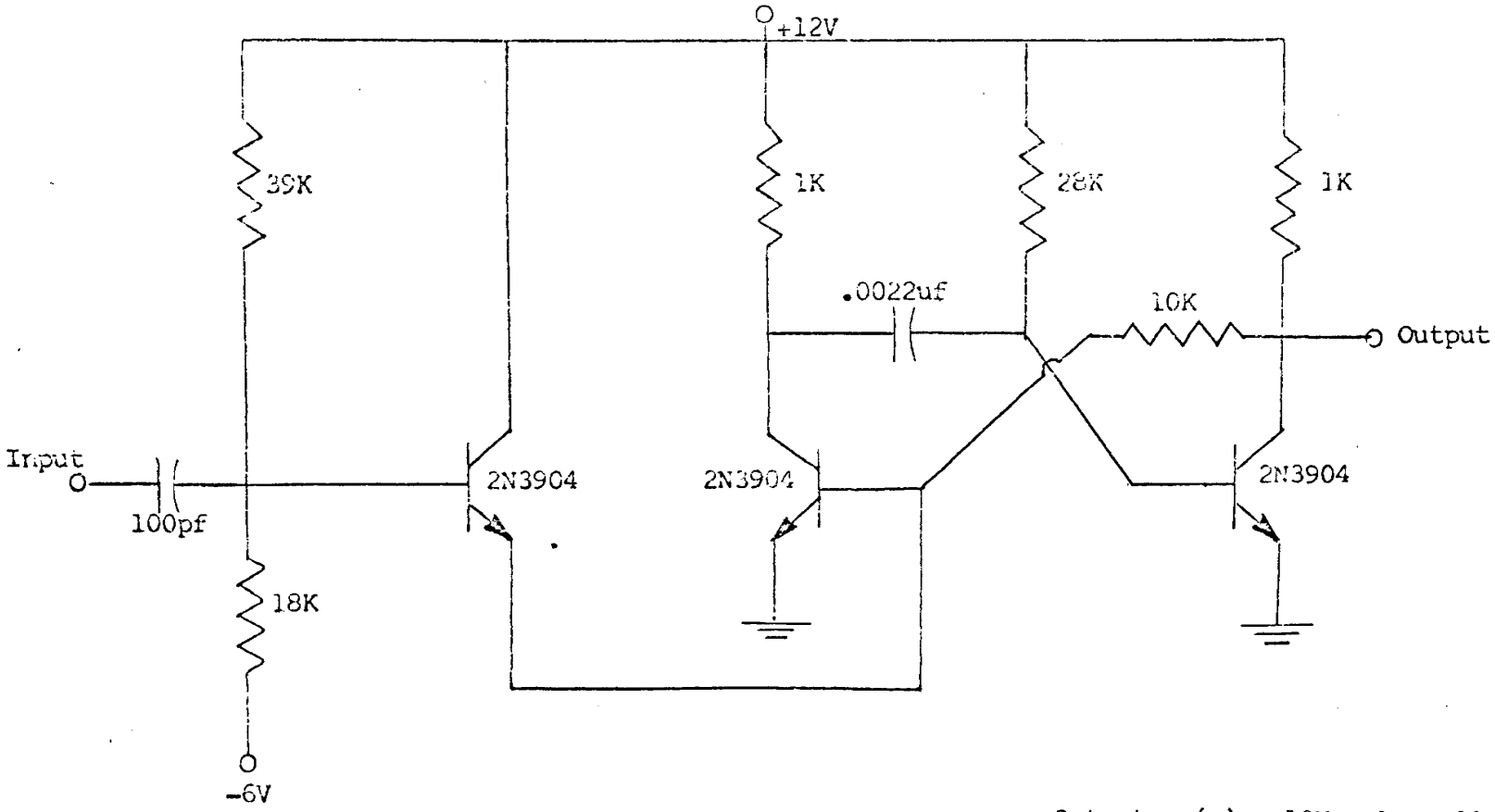
Figure 13. Logic Level Converter (-6,0 from the controller into +8,0 of the computer)

2. One-Shot and Level Converter

A special circuit was needed to produce an output pulse of fixed duration and level for an input pulse whose duration varied over a wide range (see Figure 14). The input to this circuit is capacitively coupled to trigger only on a -6V to 0V transition. Its output is a +10V, 32 microsecond pulse capable of driving a 2.2K load. These one-shots drive the tape deck's write-step motor and also initiate both the End of File and the End of Record Gaps.

3. Electronic Switch

Two of these switches are used to externally connect either the Remote Read Select or the Remote Write Select signal to a +10V (approximate) power source. (See Figure 15.) When the input goes from 0V to -6V there is continuity between the +12 volt supply and the Write (or Read) Select terminal. This configuration is capable of handling a 200 milliampere current as specified by the tape deck manual. When the input is at 0V an almost perfect open circuit exists between the



Input: (a) can be either a pulse or level

(b) triggers the circuit on the leading edge

(c) may be reapplied during the output time without effect

Output: (a) +10V pulse, 32 usec. wide

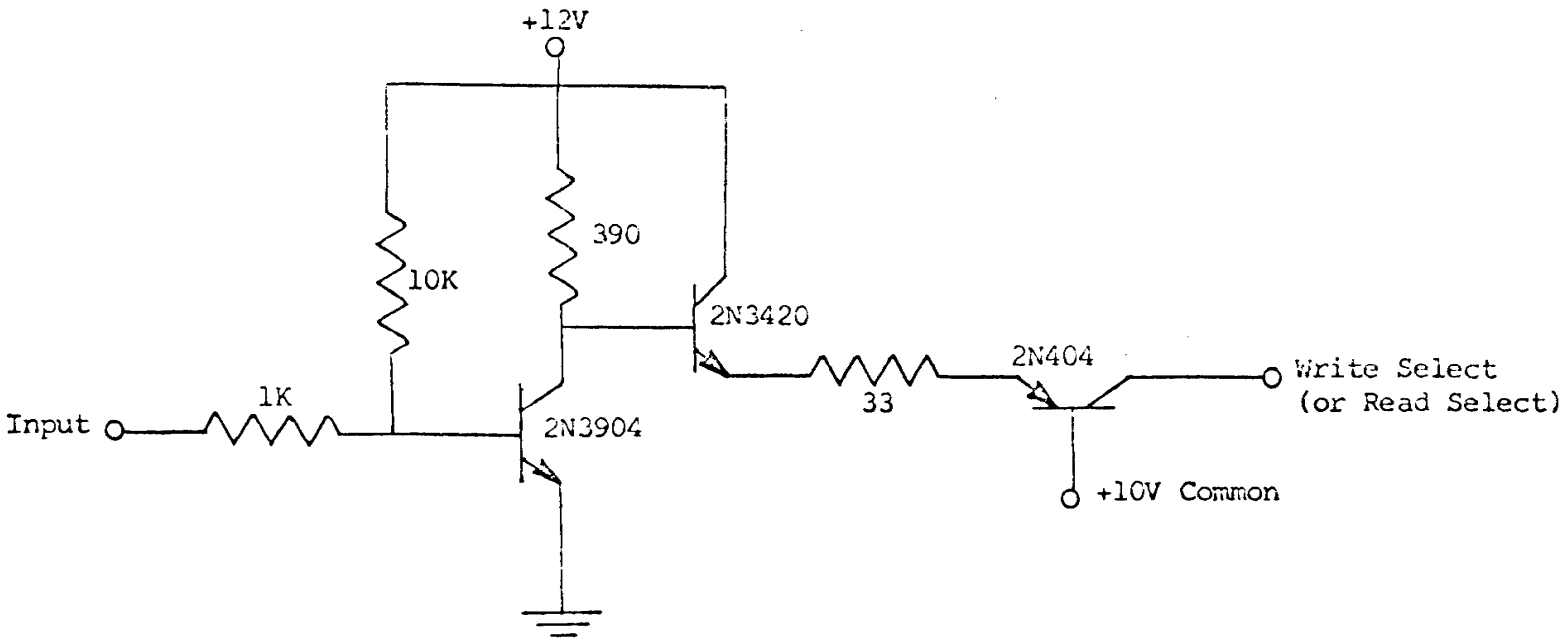
(b) 0.4 usec. rise time

(c) 0.8 usec. fall time

(d) feeds a 2.2K load

Figure 14. One-Shot and Level Converter

+12V supply and the Write (or Read) Select terminal.



Operation:

When the input goes from 0V to -6V the two leads specified (from tape deck) will be connected and remain so until the input returns to 0V. The output transistor will handle the 200 milliamperes specified by the tpae deck manual.

Figure 15. Electronic Switch

APPENDIX C

Tape Deck and Computer Signals

Figure 16 is a block diagram of the system interfaces. It shows how output signals originating in the tape unit and the computer are brought together in the S-Pac cabinet where the S-Pac logic cards are then used to control these signals and send the appropriate inputs back to either the tape deck or computer terminal.

Connections between these various interfaces are listed in Table I through Table VI. The Kennedy Tape Deck signals are described in detail in the notes following Table I and Table III. Descriptions of the SCC-650 computer signals can be found in the S.C.C. Interface Description Manual.

Table VII contains a listing of all the abbreviations used in the signal lists as well as those used in the logic diagrams.

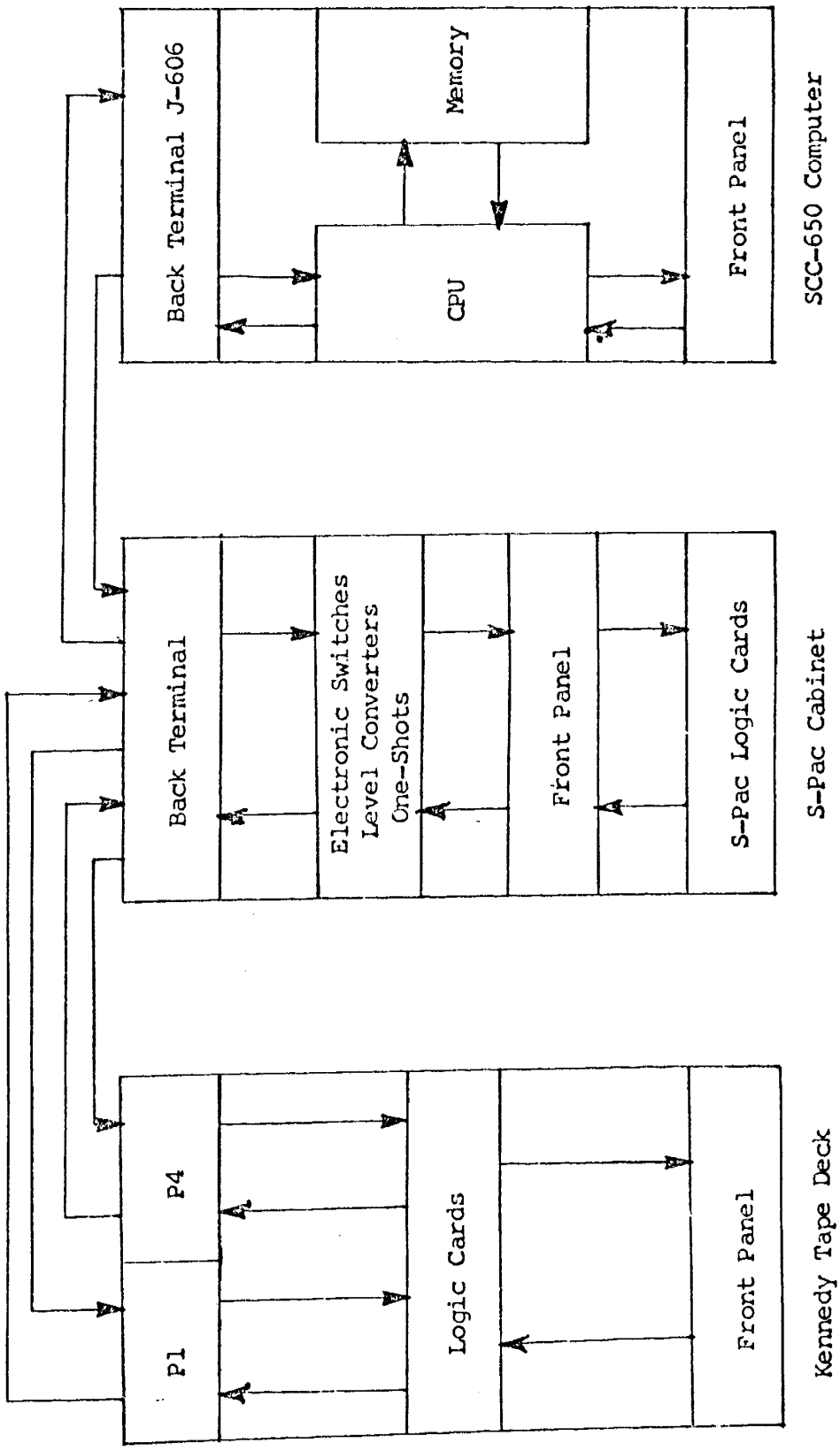


Figure 16. System Interfaces

Kennedy Tape Deck Write Signals	Tape Deck Connector P1	S-Pac Back Terminal
End of Record Input (1) (2)	P1-A	B-15
End of File Input (1) (3)	P1-B	B-16
Write-Step Input (1) (4)	P1-C	B-17
Ready Output (5)	P1-D	A-09
Echo Check Output, Channel 2 (6)	P1-E	NOT USED
Remote Load-Forward (4) (7)	P1-F	A-07
Signal Ground (8)	P1-G	C-02
Data Input, Channel 1 (9)	P1-H	A-01
Data Input, Channel 2 (9)	P1-J	A-02
Data Input, Channel 4 (9)	P1-K	A-03
Data Input, Channel 8 (9)	P1-L	A-04
Data Input, Channel A (9)	P1-M	A-05
Data Input, Channel B (9)	P1-N	A-06
Echo Check Output, Channel 1 (6)	P1-P	NOT USED
Remote Reset (1) (10)	P1-R	NOT USED
Echo Check Output, Channel 4 (6)	P1-S	NOT USED
Echo Check Output, Channel 8 (6)	P1-T	NOT USED
Echo Check Output, Channel A (6)	P1-U	NOT USED
Echo Check Output, Channel B (6)	P1-V	NOT USED
Echo Check Output, Channel C (6)	P1-W	NOT USED
Echo Parity Check Output (11)	P1-X	D-18
End of Tape Output (12)	P1-Y	A-10

Table I. Connection List for Kennedy Tape Deck Write Signals between Tape and S-Pac Back Terminals

Kennedy Tape Deck Write Signals	Tape Deck Connector P1	S-Pac Back Terminal
Load Point Output (13)	P1-Z	A-11
Broken Tape Output (14)	P1-a	A-12
Remote Ready (15)	P1-b	NOT USED
Remote Rewind (16)	P1-c	B-18
Parity Out/Data In, Channel C (17)	P1-d	A-13
Gap in Process Output (18)	P1-e	A-14
-10 volts (19)	P1-f	NOT USED
+10 volts (19)	P1-g	NOT USED
Chassis Ground (8)	P1-h	C-03
Reverse Level (20)	P1-l	A-08
Remote Load-Forward (21)	P1-m	NOT USED

Table I. Connection List for Kennedy Tape Deck Write Signals between Tape and S-Pac Back Terminals (continued)

NOTES:

1. Pulse input to tape deck, V_1=+10V, V_0=0V to 0.5V, pulse duration of 32 microseconds, rise time of 0.4 microseconds, fall time of 0.8 microseconds.

2. This pulse initiates a 0.75 inch record gap. The Gap in Process Output signal drops to 0 volts while the gap is being generated.

3. This pulse initiates a 3.4 inch gap containing a file mark (binary 60) and its longitudinal check character followed by a 0.75 inch gap. The Gap in Process Output signal drops to 0 volts while the gap is being generated.

4. The Write-Step Input and the Remote Load-Forward signals must not be applied simultaneously.

5. Output level, V_1=+10V (low impedance), V_0=0V to 0.5V. This output is 0V as long as the beginning of tape marker (BOT) isn't sensed by the photocell. It is +10V after the BOT is sensed and remains at this level during all input commands except Rewind. CAUTION: Do <u>not</u> short this output to ground.

6. Output pulse, V_1=+10V through Z_0=1K, V_0=0V to + 0.5V, pulse duration of 20 microseconds, rise and fall time less than 2 microseconds. Echo outputs from Data Channels 1 thru 8 are used to generate an Echo Parity character, which is then compared with the Echo Check output of Channel C in an

Exclusive OR circuit which indicates FALSE for like inputs and TRUE for unlike inputs. The output of the Exclusive OR circuit is brought out as the Echo Check Output. These signals are brought out for use in external circuit if desired.

7. Input level, V_1=+8V, V_0=0V to 0.5V, Z_{in}=10K. When this level is high, it duplicates the function of holding the Load-Forward pushbutton depressed (see Note 21).

8. Signal Ground and Chassis Ground are <u>not</u> interconnected within the unit. All grounds are shorted together on terminal strip G on the back of the S-Pac cabinet.

9. Input level, V_1=+8V, V_0=0V to 0.5V, Z_{in}=10K. Level must be applied no later than the leading edge of the Write-Step Input signal must remain applied for at least 100 microseconds thereafter.

10. This input is used to write the Longitudinal Check Character (LCC) when the recorder is operated in the synchronous (1000 steps per second) mode.

11. Pulse, V_1=+10V through Z_0=1K, V_0=0V to + 0.7V, pulse duration 15 microseconds, rise and fall time less than 2 microseconds. Output appears approximately 60 microseconds after Write-Step command is given.

12. A photo cell amplifier produces a positive D.C. level which shifts from V_0=0V to V_1=+10V when a reflective aluminum strip, which is placed on the inner portion of the magnetic tape, passes under the photo cell sensor and causes additional light to reach the photo cell.

13. Output level, V_1=+8V through Z_{out}=1K, V_0=0V to +0.5V. The load point (beginning of tape) photo cell amplifier operates in the same fashion as the End of Tape photo cell amplifier, but the reflective strip is now located on the outer portion of the tape. Output is +8V only momentarily as the beginning of tape marker is sensed.

14. Output level, V_1=+8V through Z_{out}=1K, V_0=0V to 0.5V. A photo cell sensor is located under the magnetic tape and senses the light from two exciter lamps. This light is normally blocked by the tape itself. Output goes to +8V when tape is broken.

15. Pulse, V_1=0V (into 20 milliamperes current sink), V_0=open circuit, pulse duration 32 microseconds, rise and fall time less than 2 microseconds.

16. Pulse, V_1=0V (into 5 milliamperes current sink), V_0=open circuit. External logic in the S-Pac removes the ground (necessary to initiate Rewind) as soon as the beginning of tape marker is sensed.

17. Internal vertical odd parity appears on this line for use in external circuit if desired. V_1=+8V through Z_{out}=2.2K, V_o=0V to 0.5V. Minimum Z_L=10K.

18. Level, V_1=0V to +0.5V, V_o=+10V through Z_{out}=1K. This output is normally +10V. It goes to 0V only when a gap is being generated. It therefore remains +10V at all times while in the read mode.

19. Internal power supply voltages appear on these pins. Maximum current to be drawn from either source is 150 milliamperes.

20. Level, V_1=+8V, V_o=0V to 0.5V, Z_{in}=4.7K. Level may be changed while Write-Step commands are being applied, as long as the Write-Step command does not exceed 500 pulses per second at that time. The stepper motor will operate in reverse as long as the +8V level is maintained.

21. Level, V_1=0V to 0.5V into 15 milliamperes current sink, V_o=+10V or open circuit. This line parallels the Load-Forward push-button and allows it to be duplicated remotely.

Kennedy Tape Deck Write Signals	Printed Circuit Board		S-Pac Front
	Input	Output	Panel
End of Record Input (1)	9-h	9-m	H-5
End of File Input (1)	9-K	9-P	H-6
Write-Stop Input (1)	9-F	9-L	H-7
Ready Output (2)	6-K	6-S	C-3
Echo Check Output, Channel 2	NOT USED	NOT USED	NOT USED
Remote Load-Forward (3)	5-f	5-n	C-6
Data Input, Channel 1 (3)	5-E	5-M	D-4
Data Input, Channel 2 (3)	5-D	5-L	D-3
Data Input, Channel 4 (3)	5-l	5-t	D-2
Data Input, Channel 8 (3)	5-k	5-s	D-1
Data Input, Channel A (3)	5-j	5-r	C-8
Data Input, Channel B (3)	5-h	5-p	C-7
Echo Check Output, Channel 1	NOT USED	NOT USED	NOT USED
Remote Reset (1)	NOT USED	NOT USED	NOT USED
Echo Check Output, Channel 4	NOT USED	NOT USED	NOT USED
Echo Check Output, Channel 8	NOT USED	NOT USED	NOT USED
Echo Check Output, Channel A	NOT USED	NOT USED	NOT USED
Echo Check Output, Channel B	NOT USED	NOT USED	NOT USED
Echo Check Output, Channel C	NOT USED	NOT USED	NOT USED
Echo Parity Check Output	3-e	3-m	F-5
End of Tape Output (2)	6-J	6-R	C-4
Load Point Output (2)	6-H	6-P	C-2

Table II. Connection List for Kennedy Tape Deck Write Signals between Printed Circuit Boards and S-Pac Front Panel

Kennedy Tape Deck Write Signals	Printed Circuit Board		S-Pac Front Panel
	Input	Output	
Broken Tape Output (2)	6-F	6-N	C-1
Remote Ready	8-k	8-s	I-6
Remote Rewind (4)	8-j	8-r	H-8
Parity Out/Data In, Channel C (2)	6-E	6-M	B-8
Gap in Process Output (2)	6-D	6-L	B-7
Reverse Level (3)	5-e	5-m	C-5
Remote Load-Forward	8-i	8-t	I-3

Table II. Connection List for Kennedy Tape Deck Write Signals between Printed Circuit Boards and S-Pac Front Panel (continued)

NOTES:

1. Printed circuit board #9 contains four one-shots. (See Figure 14 for circuit description.) The input of the one-shot is connected to the S-Pac front panel while the output is connected to the back terminal.

2. Printed circuit board #6 contains twelve logic level converters. In this application a signal from the tape deck (logic levels 0V and 8V) is input into the S-Pacs (logic levels 0V and -6V). (See Figure 11 for circuit description.) The input to the level converter (base of the transistor) is connected to the back terminal while the output (collector) is connected to the front panel.

3. Printed circuit board #5 contains twelve logic level converters. In this application a signal from the S-Pacs (logic levels 0V and -6V) is input into the tape deck (logic levels 0V and +8V). (See Figure 12 for circuit description.) The input to the level converter is connected to the front panel and the output is connected to the rear terminal.

4. Printed circuit board #8 contains special circuitry. In this application 0V and open circuit are needed as outputs of a logic level converter. (See Figure 12 for circuit description.) The logic level converter is exactly like the one described in Note 3 except that the collector resistor, diode, and power supply are removed.

Kennedy Tape Deck Read Signals	Tape Deck Connector P4	S-Pack Back Terminal
Data Output, Channel 1 (1)	P4-1	A-15
Data Output, Channel 2 (1)	P4-2	A-16
Data Output, Channel 4 (1)	P4-3	A-17
Data Output, Channel 8 (1)	P4-4	A-18
Data Output, Channel A (1)	P4-5	B-01
Data Output, Channel B (1)	P4-6	B-02
Data Output, Channel C (1)	P4-7	B-03
Clock Output (2)	P4-10	B-04
Gap Detect Output (3)	P4-12	B-06
Remote Read Select (4)	P4-14	B-11
Remote Write Select (4)	P4-15	B-12
Select Common (5)	P4-16	B-13
File Protect Output (6)	P4-17	B-07
Write Status (7)	P4-18	B-08
Read Status (7)	P4-19	B-09
Remote Status (7)	P4-20	B-10
Longitudinal Check Character (8)	P4-21	NOT USED
Longitudinal Check Character (8)	P4-22	NOT USED
Signal Ground (9)	P4-35	G-03
Chassis Ground (9)	P4-36	G-04

Table III. Connection List for Kennedy Tape Deck Read Signals between Tape and S-Pac Back Terminals

NOTES:

1. Pulse, V_1=+10V through Z_{out}=1K, V_o=0V to + 0.5V, 20 microsecond pulse duration, rise and fall time less than 2 microseconds. Pulses coincide with the Read Clock Output signal.

2. Pulse, V_1=+10V through Z_{out}=1K, V_o=0V to + 0.5V, 20 microsecond pulse duration, rise and fall time less than 2 microseconds. Pulses coincide with the pulses on the data lines.

3. Level, V_1=0V to + 0.5V, V_o=+10V through Z_{out}=1K. This output goes to +10V when a blank more than two character spacings in width is read. Assuming data in the standard format is being read, the gap detector output will be positive during the block; it will drop to zero between the end of the block and the Longitudinal Check Character. Upon reading the LCC, output will again rise and then fall as the interrecord gap is entered. The LCC appears at the data output.

4. The Remote Write Select and the Remote Read Select signals are used in conjunction with the Selector Common output signal (see Note 5) whenever the front panel Write-Read-Remote switch is in the Remote position. In any other position of the front panel switch, these inputs are open circuits.

5. Level, V_1=+10V (low impedance), V_o=0V to + 0.5V. V_1 appears whenever Ready Output (on P1) is present. This line must be externally switched into either Remote Read or Remote Write Select

input (not simultaneously) to control these functions remotely whenever the front panel Write-Read-Remote switch is in the Remote position. Current through the external switch will not exceed 200 milliamperes. CAUTION: Do not short this line to ground.

6. Level, V_1=+10V (low impedance), V_o=0V to + 0.5V. A file protect switch is located under the left tape reel. If a file protect ring is on this reel, the switch will be depressed, the File Protect Output will be V_o, and both reading and writing are possible. V_1 appears whenever writing is attempted without the file protect ring. (The tape cannot be written on with the file protect ring off.) CAUTION: Do not short-circuit this line to ground.

7. Read, Write, or Remote Status line is connected to signal ground, depending on position of selector switch on front of unit. If not connected to ground these inputs appear as open circuits.

8. To inhibit the output of the Longitudinal Check Character connect P4-21 to P4-22.

9. Signal Ground and Chassis Ground are not interconnected within the unit. All grounds are shorted together on terminal strip G on the back of the S-Pac cabinet.

Kennedy Tape Deck Read Signals	Printed Circuit Board		S-Pac Front Panel
	Input	Output	
Data Output, Channel 1 (1)	6-l	6-t	B-2
Data Output, Channel 2 (1)	6-k	6-s	B-1
Data Output, Channel 4 (1)	6-j	6-r	B-3
Data Output, Channel 8 (1)	6-h	6-p	B-4
Data Output, Channel A (1)	6-f	6-n	B-5
Data Output, Channel B (1)	6-e	6-m	B-6
Data Output, Channel C (1)	7-K	7-S	A-8
Clock Output (1)	7-J	7-R	A-7
Gap Detect Output (1)	7-F	7-N	A-5
Remote Read Select (2)	8-K	8-H	H-1
Remote Write Select (2)	8-F	8-D	H-2
File Protect Output (1)	7-E	7-M	A-4
Write Status (3)	7-D	7-L	A-3
Read Status (3)	7-l	7-t	A-2
Remote Status (3)	7-k	7-s	A-1

Table IV. Connection List for Kennedy Tape Deck Read Signals between Printed Circuit Boards and S-Pac Front Panel

NOTES:

1. Printed circuit boards #6 and #7 each contain twelve logic level converters. In this application a signal from the tape deck (logic levels 0V and +8V) is input into the S-Pacs (logic levels 0V and -6V). (See Figure 11 for circuit description.) The input to the level converter (base of the transistor) is connected to the back terminal while the output (collector) is connected to the front panel.

2. Two electronic switches (see Figure 15) are provided on printed circuit board #8 to allow the +10V common line to be shorted to either Write or Read Select. The input to this circuit is available on the front panel while the outputs go to the rear terminal.

3. Biasing on three of the level converters on circuit board #7 was changed to allow the level converter to distinguish between open circuit and ground at its input.

SCC-650 Computer Signals	Function	Computer J-606	S-Pac Back Terminal
IN00-	Accumulator Input	A	E-01
IN01-	" "	B	E-02
IN02-	" "	C	E-03
IN03-	" "	D	E-04
IN04-	" "	E	E-05
IN05-	" "	F	E-06
IN06-	" "	H	E-07
IN07-	" "	J	E-08
IN08-	" "	K	E-09
IN09-	" "	L	E-10
IN10-	" "	M	E-11
IN11-	" "	N	E-12
AC00B-	Accumulator Output	P	C-01
AC01B-	" "	R	C-02
AC02B-	" "	S	C-03
AC03B-	" "	T	C-04
AC04B-	" "	U	C-05
AC05B-	" "	V	C-06
AC06B-	" "	W	C-07
AC07B-	" "	X	C-08
AC08B-	" "	Y	C-09
AC09B-	" "	Z	C-10

Table V. Connection List for SCC-650 Computer Signals between Computer and S-Pac Back Terminals

SCC-650 Computer Signals	Function	Computer J-606	S-Pac Back Terminal
AC10B-	Accumulator Output	a	C-11
AC11B-	" "	b	C-12
ZEROB082	Signal Ground	c	G-05
ZEROB083	" "	d	G-06
ZEROB081	" "	e	G-07
ZEROB081	" "	f	G-08
R04B-	Instruc. Reg. Output	h	C-13
R05B-	" " "	j	C-14
R06B-	" " "	k	C-15
R07B-	" " "	l	C-16
R08B-	" " "	m	C-17
R09B-	" " "	n	C-18
R10B-	" " "	p	D-01
R11B-	" " "	r	D-02
IOE-	I/O Error	s	E-13
		t	
RT1B-	Timing Pulse	u	D-14
RT3B-	" "	v	D-15
RT4B-	" "	w	D-05
RT5B-	" "	x	D-16
RT7B-	" "	y	D-17
STCLEAR-	Start Clear	z	D-13

Table V. Connection List for SCC-650 Computer Signals between Computer and S-Pac Back Terminals (continued)

SCC-650 Computer Signals	Function	Computer J-606	S-Pac Back Terminal
EXTINT-	External Interrupt	AA	E-14
SDFB-	Skip on Device Flag	BB	D-07
DSTB-	Input Device Status	CC	D-08
TFAB-	Transfer from Accumulator	DD	D-09
TTAB-	Transfer to Accumulator	EE	D-10
DRDYB-	Device Ready (Output)	FF	D-11
RT0B-	Timing Pulse	HH	D-03
RT2B-	" "	JJ	D-04
RT6B-	" "	KK	D-06
IOPB-	I/O Instruction	LL	D-12
DF-	Device Flag	MM	E-15
IDRBX-	Device Ready (Input)	NN	E-16

Table V. Connection List for SCC-650 Computer Signals between Computer and S-Pac Back Terminals (continued)

SCC-650 Computer Signals	Printed Circuit Board		S-Pac Front
	Input	Output	Panel
IN00-	4-K	4-S	F-4
IN01-	4-J	4-R	F-3
IN02-	4-H	4-P	F-2
IN03-	4-F	4-N	F-1
IN04-	4-E	4-M	E-1
IN05-	4-D	4-L	E-2
IN06-	4-l	4-t	E-3
IN07-	4-k	4-s	E-4
IN08-	4-j	4-r	E-5
IN09-	4-h	4-p	E-6
IN10-	4-f	4-n	E-7
IN11-	4-e	4-m	E-8
AC00B-	1-K	1-S	J-1
AC01B-	1-J	1-R	J-2
AC02B-	1-H	1-P	J-3
AC03B-	1-F	1-N	J-4
AC04B-	1-E	1-M	J-5
AC05B-	1-D	1-L	J-6
AC06B-	1-l	1-t	J-7
AC07B-	1-k	1-s	J-8
AC08B-	1-j	1-r	K-8
AC09B-	1-h	1-p	K-7

Table VI. Connection List for SCC-650 Computer Signals between Printed Circuit Boards and S-Pac Front Panel

SCC-650 Computer Signals	Printed Circuit Board		S-Pac Front
	Input	Output	Panel
ACl0B-	1-f	1-n	K-6
ACl1B-	1-e	1-m	K-5
R04B-	2-K	2-S	K-4
R05B-	2-J	2-R	K-3
R06B-	2-H	2-P	K-2
R07B-	2-F	2-N	K-1
R08B-	2-E	2-M	L-1
R09B-	2-D	2-L	L-2
R10B-	2-l	2-t	L-3
R11B-	2-k	2-s	L-4
ICE-	5-K	5-S	D-8
RT1B-	3-k	3-s	G-8
RT3B-	3-j	3-r	F-6
RT4B-	2-f	2-n	L-7
RT5B-	3-h	3-p	F-7
RT7B-	3-f	3-n	F-8
STCLEAR-	3-l	3-t	G-7
EXTINT-	5-J	5-R	D-7
SDFB-	3-K	3-S	G-1
DSTB-	3-J	3-R	G-2
TFAB-	3-H	3-P	G-3
TTAB-	3-F	3-N	G-4

Table VI. Connection List for SCC-650 Computer Signals between Printed Circuit Boards and S-Pac Front Panel (continued)

SCC-650 Computer Signals	Printed Circuit Board		S-Pac Front Panel
	Input	Output	
DRDYB-	3-E	3-M	G-5
RTOB-	2-j	2-r	L-5
RT2B-	2-h	2-p	L-6
RT6B-	2-e	2-m	L-8
IOPB-	3-D	3-L	G-6
DF-	5-H	5-P	D-6
IDRDY-	5-F	5-N	D-5

Table VI. Connection List for SCC-650 Computer Signals between Printed Circuit Boards and S-Pac Front Panel (continued)

Signal	Description
AC00-AC11	12 Bit Accumulator Output
BTOUT	Broken Tape Output
CLRTBR	Clear Tape Buffer Register
DATIN	Data Input to Computer
DF	Device Flag Signal to Computer
DIC1-DICB	6 Data Input Channels to Tape Deck
DOC1-DOCB	6 Data Output Channels from Tape Deck
DRDY	Device Ready Output from Computer
DST	Device Status Command
DSTDTA	Device Status Data to Computer
DTAOUT	Data Output from Computer
DTTR1	First Six-bit Transfer onto Tape
DTTR2	Second Six-bit Transfer onto Tape
EOTOUT	End of Tape Output
EPCOUT	Echo Parity Check Output
EXTINT	External Interrupt
EXU	Execute Command
EXUAC	Execute Accumulator's Contents
FPOUT	File Protect Output
GAPFF	Gap Flip-Flop
GAPIP	Gap in Process (during Writing)
GPDOUT	Gap Detect Output (during Reading)
IDRDY	Input Device Ready

Table VII. List of Abbreviations

Signal	Description
IN00-IN11	12 Bit Accumulator Input
IOE	Input-Output Error
IOP	Input-Output Instruction
LFMRFF	Load-Forward Make Ready Flip-Flop
LPOUT	Load Point Output
MAGTP	Magnetic Tape (MAGTPR + MAGTPW)
MAGTPR	Magnetic Tape Read (decode of R07...R11)
MAGTPW	Magnetic Tape Write (decode of R07...R11)
MTPRSL	Magnetic Tape Read Select
MTPWSL	Magnetic Tape Write Select
MTPWT6	(Magnetic Tape Write)*(T6)
NTCP	Narrow Tape Clock Pulse (3 usec.)
R04-R11	8 Bits of the Instruction Register
RDYAG1	Ready Again for the First Time Flip-Flop
RDYAG2	Ready Again for the Second Time Flip-Flop
RDYOUT	Ready Output
RLFWD	Remote Load Forward
RMRDY	Remote Ready
RMSTAT	Remote Status
RRDYFF	Reset Ready Flip-Flop
RRWD	Remote Rewind
RSTAT	Read Status
RSTP	Reverse Stepper

Table VII. List of Abbreviations (continued)

Signal	Description
SEL	Select Command
SDF	Skip on Device Flag Command
SRDYFF	Set Ready Flip-Flop
STCLEAR	Start, Clear all Flip-Flops
T0-T6	Computer Clock Pulses
TBR00-TBR11	12 Bit Tape Buffer Register
TFA	Transfer from Accumulator Command
TFAFF	Transfer from Accumulator Flip-Flop
TMRCLR	Terminate, Clear all Flip-Flops
TPRDY	Tape Ready Flip-Flop
TMR	Terminate Command
TR	Transfer (TR1 + TR2)
TR1	First Transfer Flip-Flop
TR2	Second Transfer Flip-Flop
TRANSF	Transfer (TFA + TTA)
TTA	Transfer to Accumulator Command
TTADT1	Transfer to Accumulator, First Data Transfer
TTADT2	Transfer to Accumulator, Second Data Transfer
TTAFF	Transfer to Accumulator Flip-Flop
TTARLF	TTA Remote Load Forward Flip-Flop
WSTAT	Write Status
WTCP	Wide Tape Clock Pulse

Table VII. List of Abbreviations (continued)

APPENDIX D

Logic Design Information

1. Logic Diagrams

The complete logic diagrams for the Kennedy Tape Deck controller appear on pages 58 to 78.

2. TFA Description (See Figure 17.)

When the tape deck is initially selected to write, all flip-flops in the controller are cleared. The Magnetic Tape Write Select flip-flop (MTFWSL) and the Tape Ready flip-flop (TPRDY) are then set. The MTFWSL flip-flop will remain set at all times while the tape unit is in the write mode. The TPRDY flip-flop, however, will only be set when the controller is ready to receive data from the computer. As soon as the first TFA command is decoded an IDRDY (Input Device Ready) signal is sent to the computer, which acknowledges that it received this signal by sending a DRDY (Output Device Ready) signal back to the controller. This signal then conditions the 12-bit transfer from the accumulator to the tape buffer register; it also pulses the counter flip-flops (TR1 and TR2) setting TR1 and conditioning the first six-bit transfer onto tape. At T6 (a computer clock pulse) of the same TFA command the TPRDY flip-flop is rest. The IDRDY signal now indicates that the controller is no longer ready. Then 3.5 milliseconds after the TPRDY flip-flop has been reset, the counter flip-flops are again pulsed. This time TR2 is set and TR1 is reset and the second six-bit transfer is conditioned. Finally after another 3.5 milliseconds delay the TPRDY flip-flop is again set. The tape buffer register has also been cleared and the TFA cycle is ready to repeat itself if another transfer command is given.

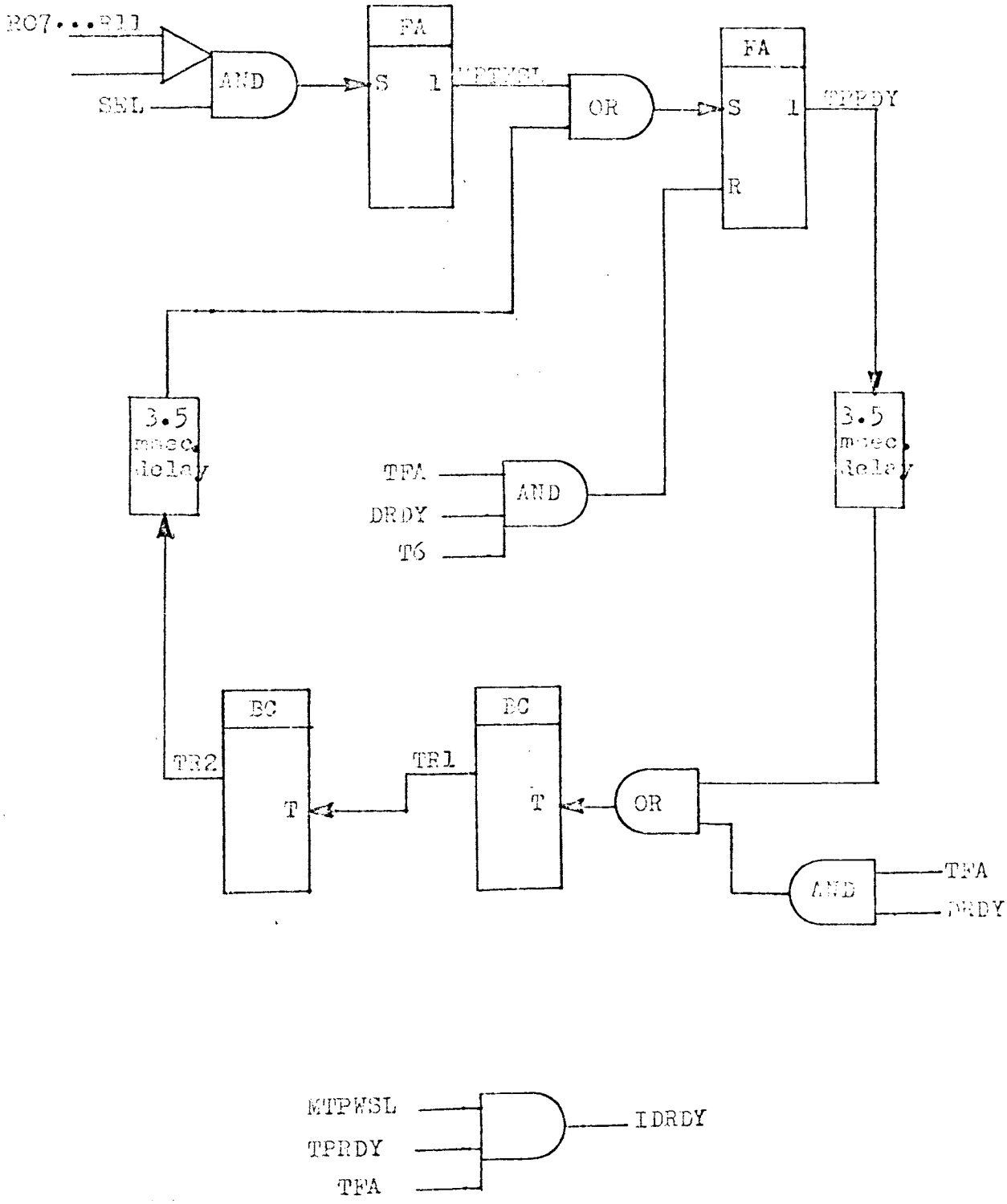


Figure 17. Simplified Delay Loop for TFA Command

The TFA command has been designed to work in the clock-step mode as a convenience to understanding as well as to troubleshooting. The two 3.5 millisecond delays will naturally be unnecessary in this mode of operation. As a result the two flip-flops (RDYAG1 and RDYAG2) will operate slightly differently in clock step. The program and explanation appear below. (Refer to pages 58 - 78.)

```
'0734        SEL  '34
'0474        TFA  '34
'2501        JMB  *-1
'2502        JMB  *-2
```

SEL•T0: $ R register is filled $

SEL•T2: $ All flip-flops are cleared $

SEL•T4: MIPWSL ⟵ 1

SEL•T6: TPRDY ⟵ 1

SEL•T7: $ R register is cleared $

TFA•T0: $ R register is filled $, TFAFF ⟵ 1, IDRDY ⟵ 1

TFA•T3: DRDY ⟵ 1, $ Tape Buffer register is filled $

TFA•T6: TPRDY ⟵ 0 $ Conditions a 3.5 millisecond delay $, IDRDY ⟵ 0

TFA•T7: TR1 ⟵ 1, $ Data input to tape deck $

TFA•T6 + 3.5 msec. : RDYAG1 ⟵ 1

T2: TR1 ⟵ 0, TR2 ⟵ 1 $ Conditions a 3.5 millisecond delay $, $ Data input to tape deck $

T4: RDYAG1 ⟵ 0

T2 + 3.5 msec. : RDYAG2 ⟵ 1

T6: RDYAG2 ⟵ 0, TR2 ⟵ 0, TPRDY ⟵ 1, TPAFF ⟵ 0,
$ Tape Buffer register is cleared $

3. TTA Description (See Figure 18.)

When the tape deck is initially selected to read, all flip-flops in the controller are cleared. The Magnetic Tape Read Select flip-flop (MTPRSL) is then set and remains in the set condition as long as the tape deck is in the read mode. The first TTA command starts the tape moving in search of a tape clock pulse (TCP) and the six bits of information coincident with it. The first TCP pulses the counter flip-flops (TR1 and TR2) setting TR1 and conditioning the first six-bit transfer from the tape deck into the tape buffer register. The second TCP again pulses the counter flip-flops setting TR2 and resetting TR1. Six more bits are then transferred into the controller and an IDRDY signal is sent to the computer indicating that a 12-bit word has been assembled and is ready to be transferred. The next TTA command will then fill the accumulator and send a DRDY signal to the controller. This signal will reset TPRDY, TR2, and the entire tape buffer register. The cycle is now ready to repeat itself.

The timing diagram in Figure 19 provides an easy check on the circuit's performance. Alternate 12-bit words consisting of all ONES and then all ZEROS were written on the tape.

4. Location of S-Pac Cards

Table VIII contains the information necessary to locate a particular logic card in the S-Pac cabinet. The first digit of the

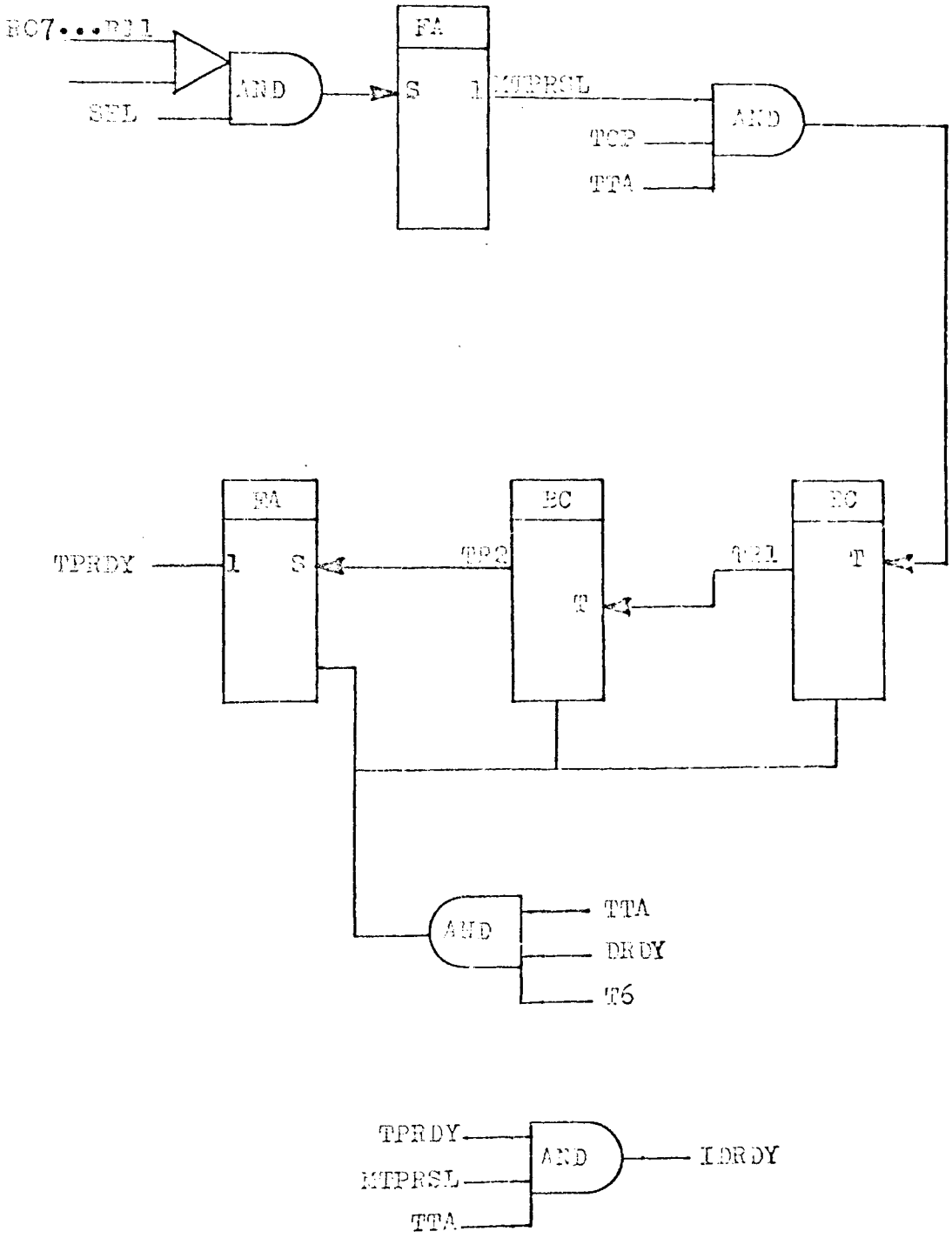


Figure 18. Simplified Delay Loop for TTA Command

three-digit location number indicates the rack (number 1 is the top rack, number 2 is the bottom rack). The next two digits indicate the slot number (there are 28 slots in each rack).

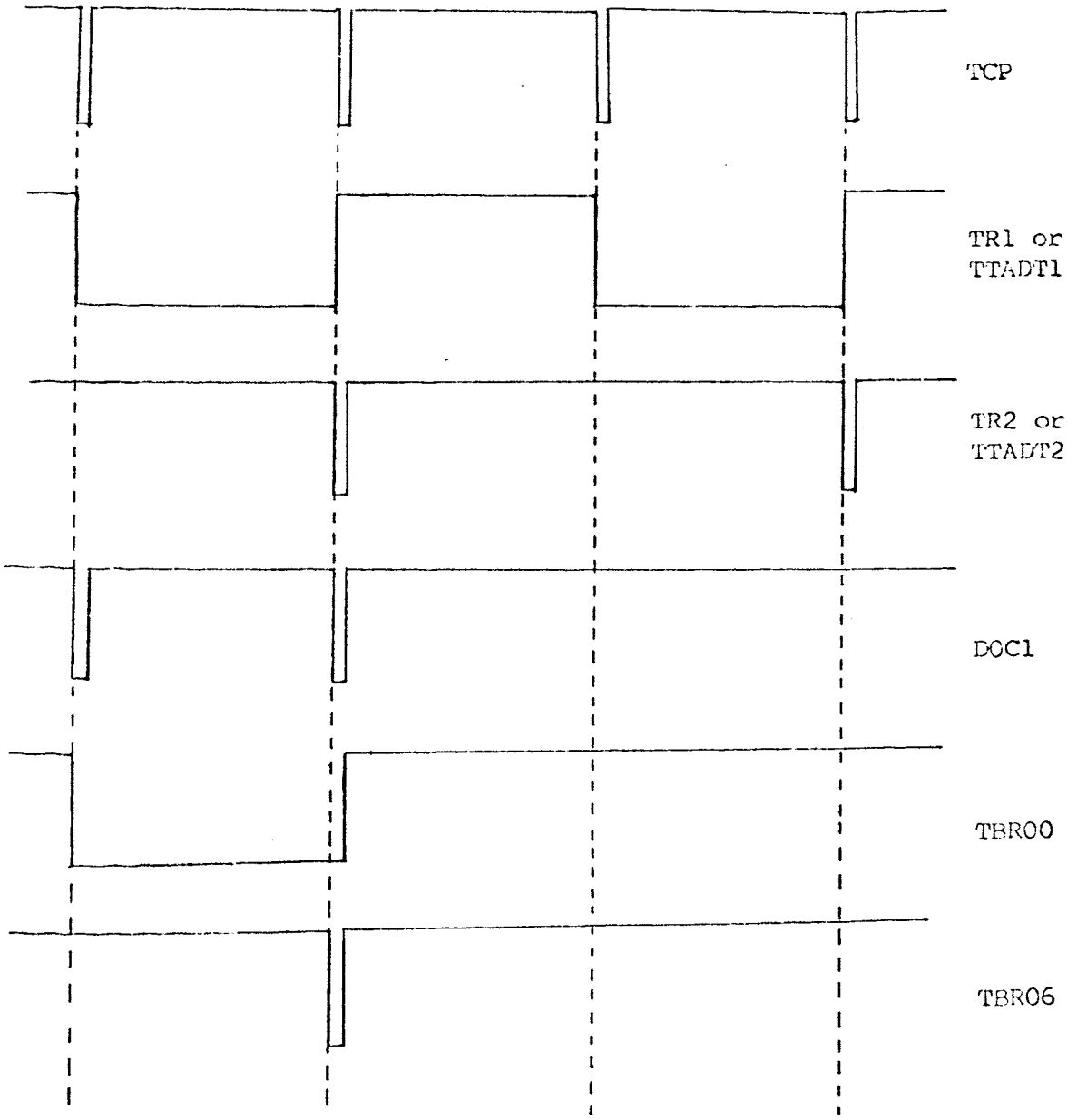
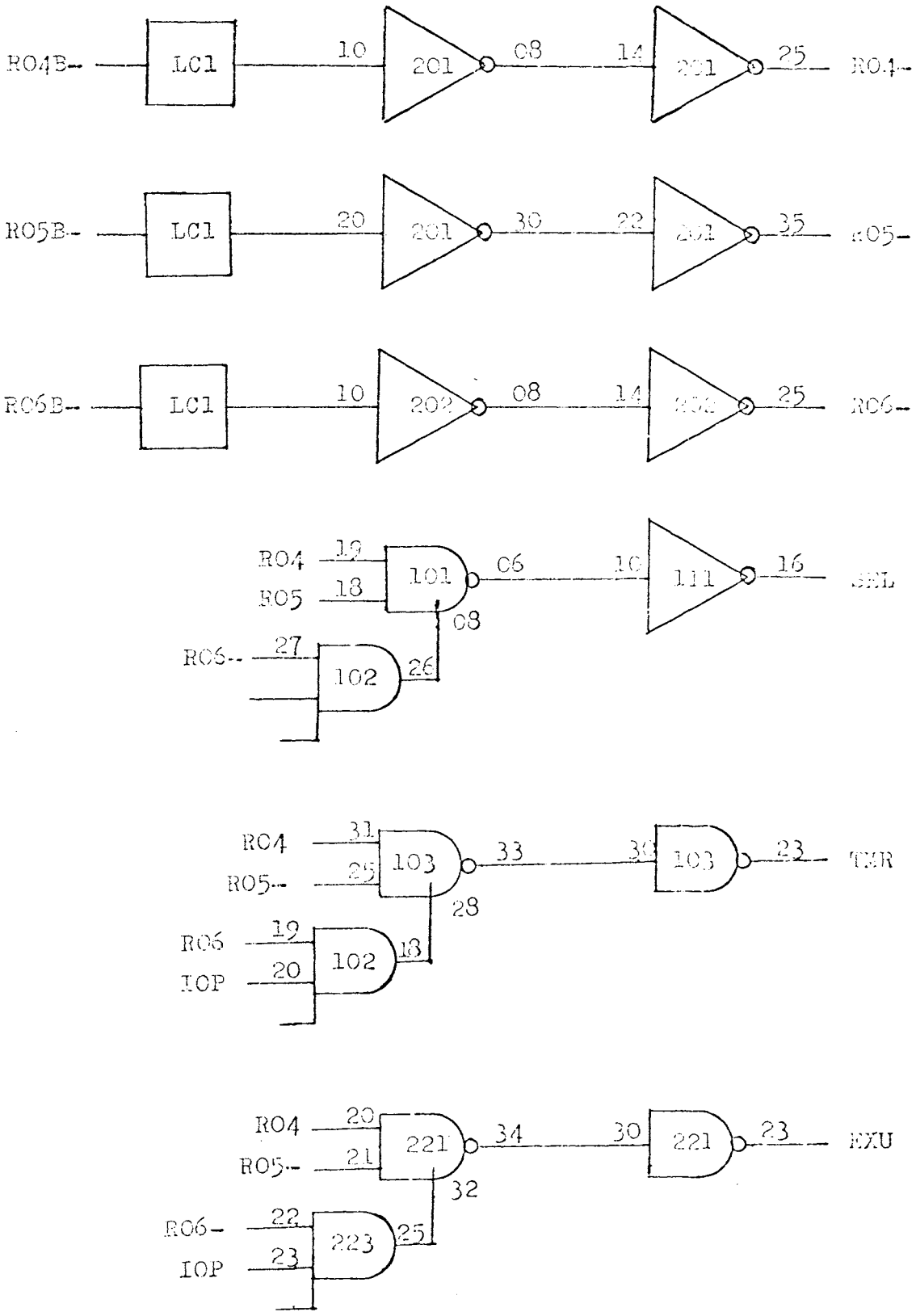
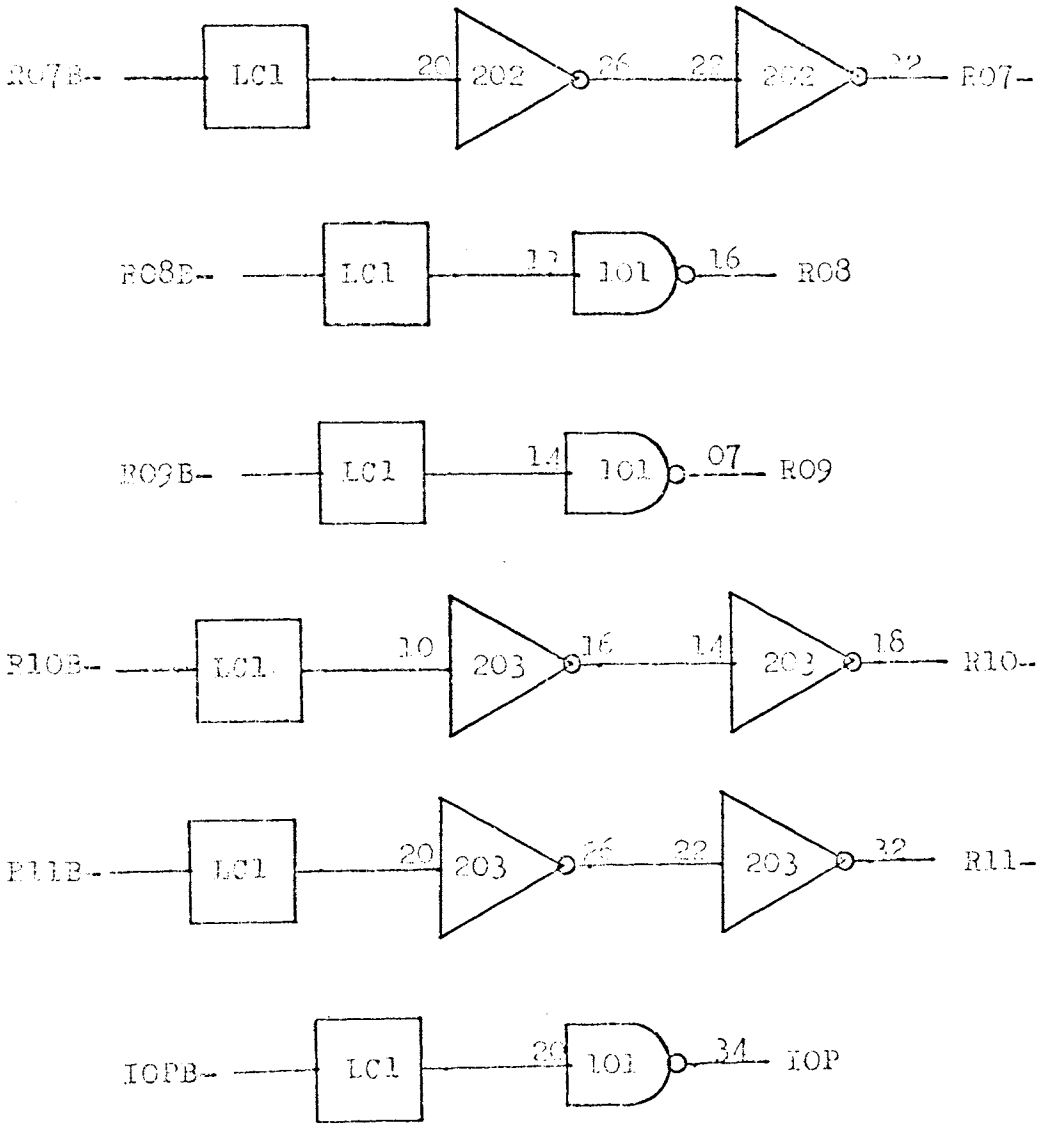
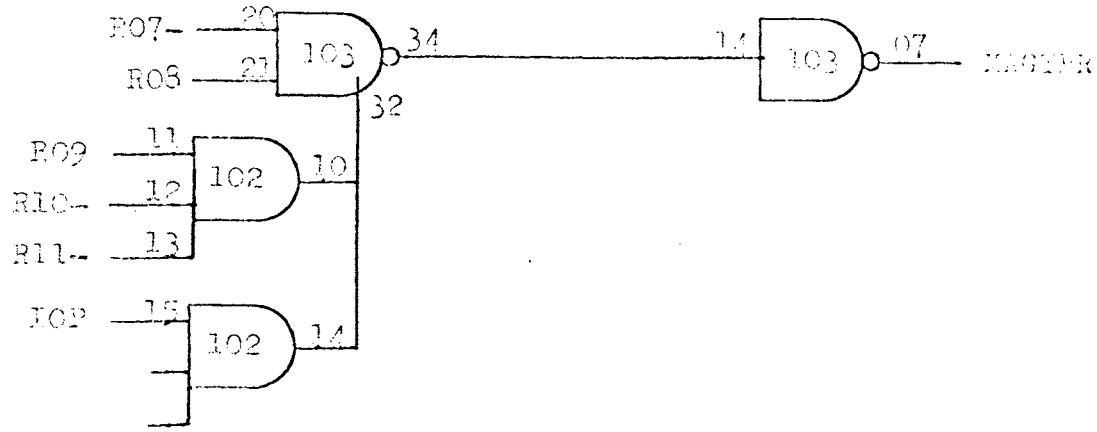
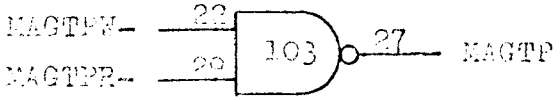


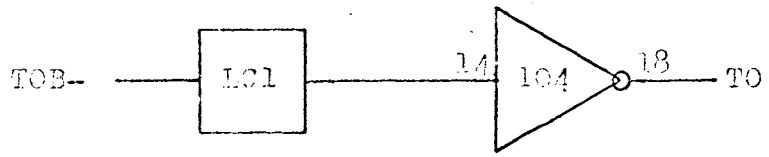
Figure 19. Timing Diagram for TTA Operation

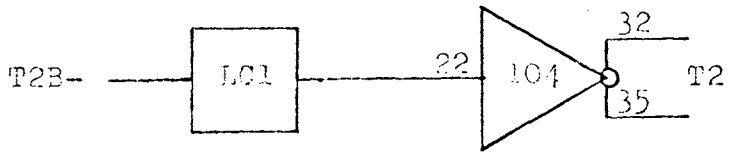

RO4B--
LC1
10
201
08
14
201
25
RO4--
RO5B--
LC1
20
201
30
22
201
35
RO5--
RO6B--
LC1
10
202
08
14
202
25
RO6--
RO4
RO5
19
18
101
06
10
111
16
SEL
08
RO6--
27
102
26
RO4
RO5--
31
25
103
33
39
103
23
TMR
28
RO6
IOP
19
20
102
18
RO4
RO5--
20
21
221
34
30
221
23
EXU
32
RO6--
IOP
22
23
223
25

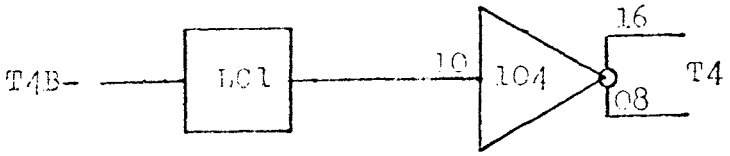

R07B--
LC1
20
202
26
22
202
32
R07--
R08B--
LC1
12
101
16
R08
R09B--
LC1
14
101
07
R09
R10B--
LC1
10
203
16
14
203
18
R10--
R11B--
LC1
20
203
26
22
203
32
R11--
IOPB--
LC1
28
101
34
IOP
R07
08
R08
02
102
06
07
31
101
33
MAGTPW
R09
31
R10--
32
102
30
R11--
34
IOP
35
102
33

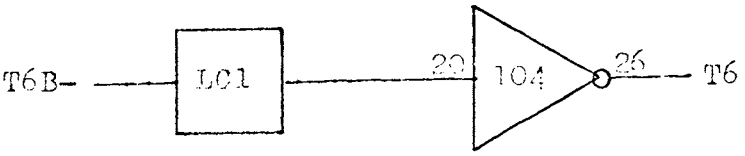

R07-
R08
20
21
103
34
32
14
103
07
R09
R10-
R11-
11
12
13
102
10
P0P
15
102
14

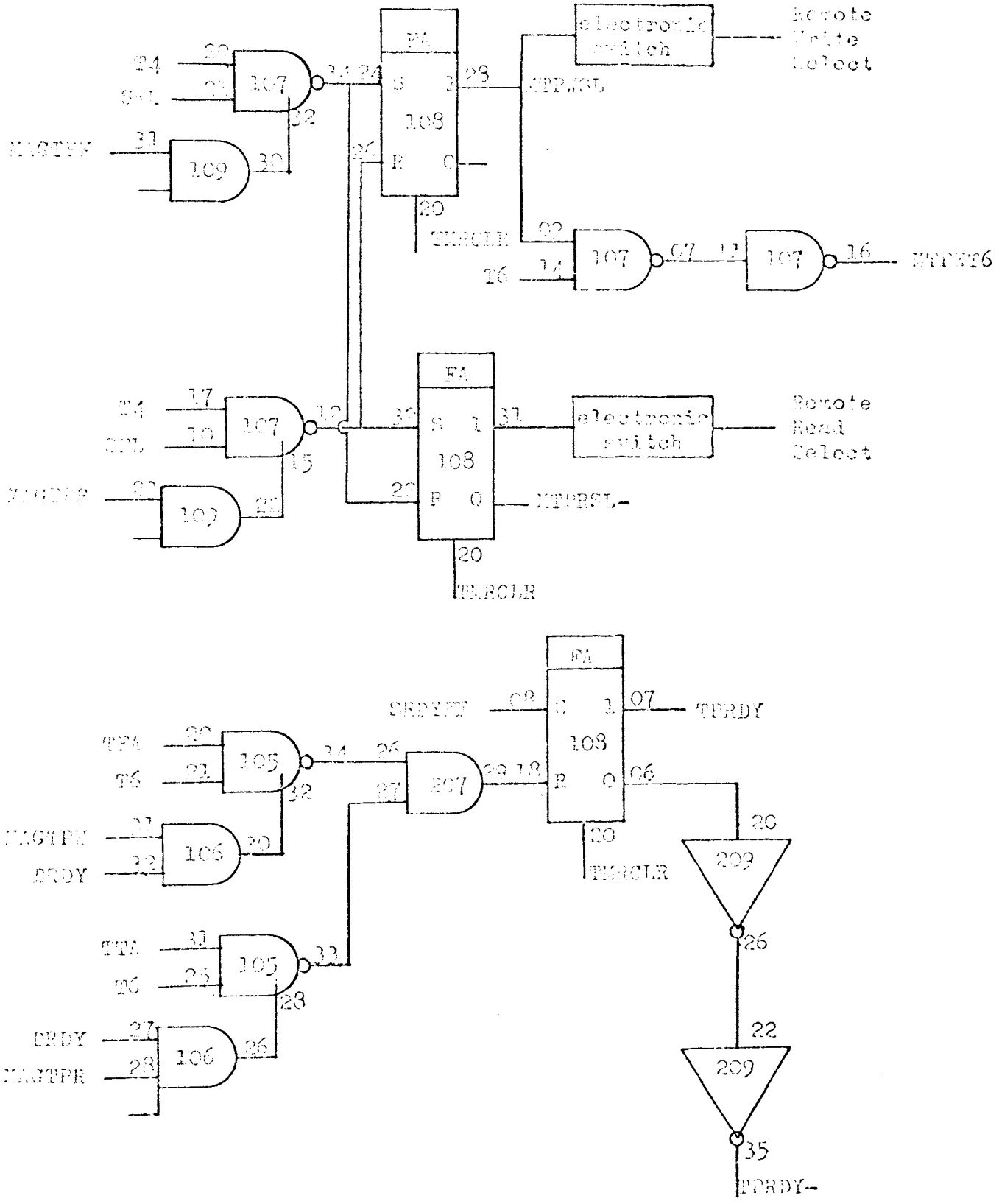

MAGTPW-
MAGTPR-
22
103
27
MAGTP

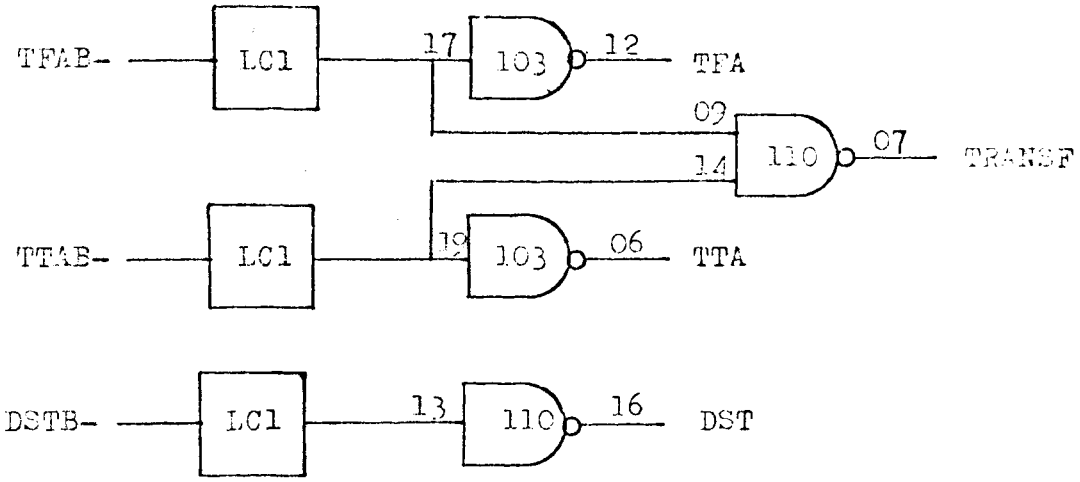

T0B-
LC1
14
104
18
T0

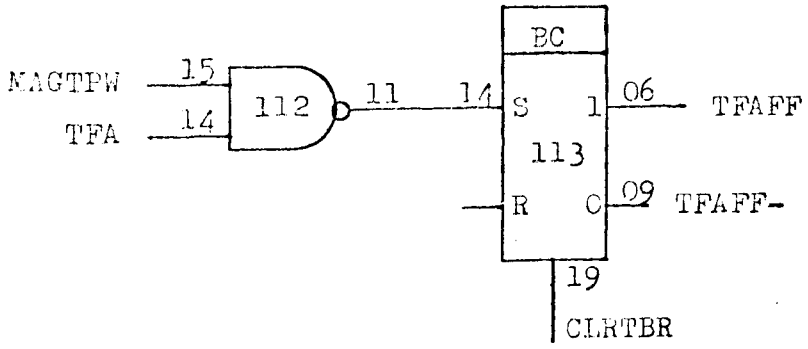

T2B-
LC1
22
104
32
35
T2

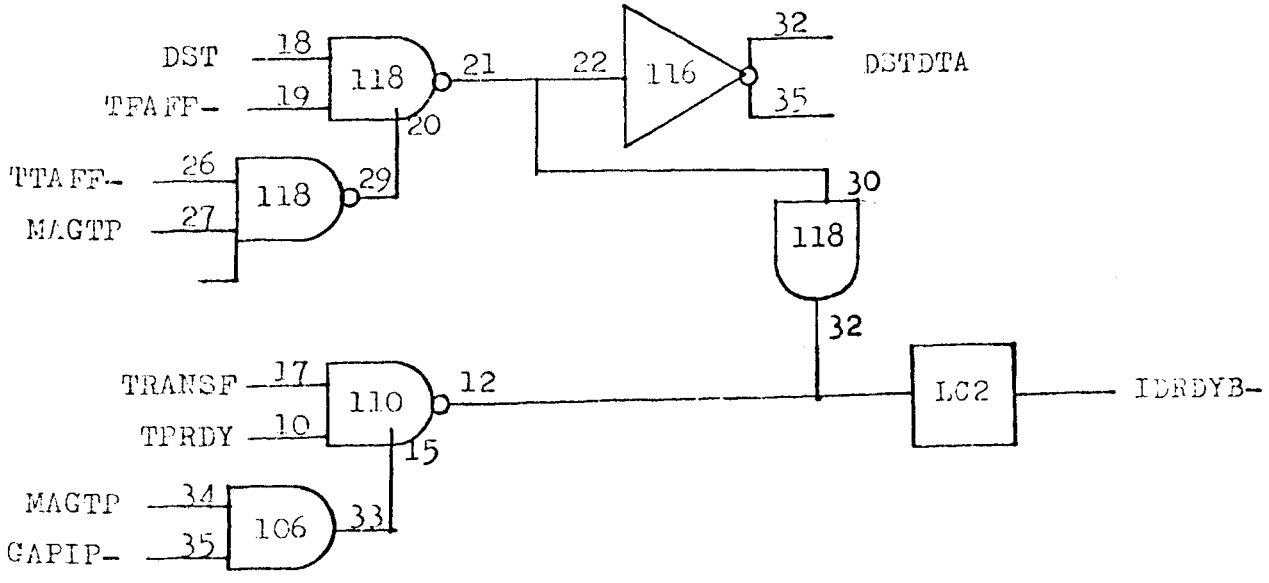

T4B-
LC1
10
104
16
08
T4

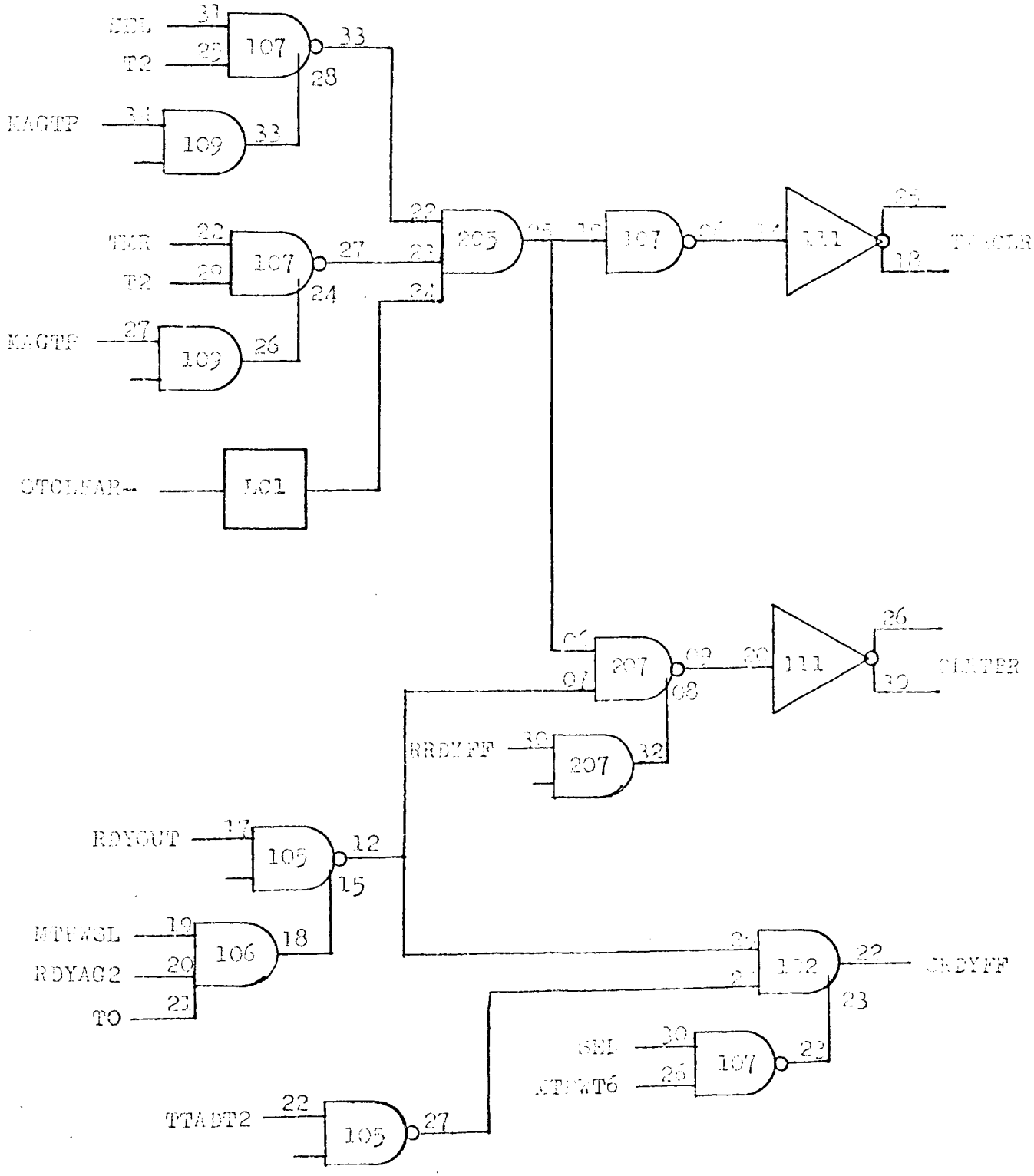

T6B-
LC1
20
104
26
T6

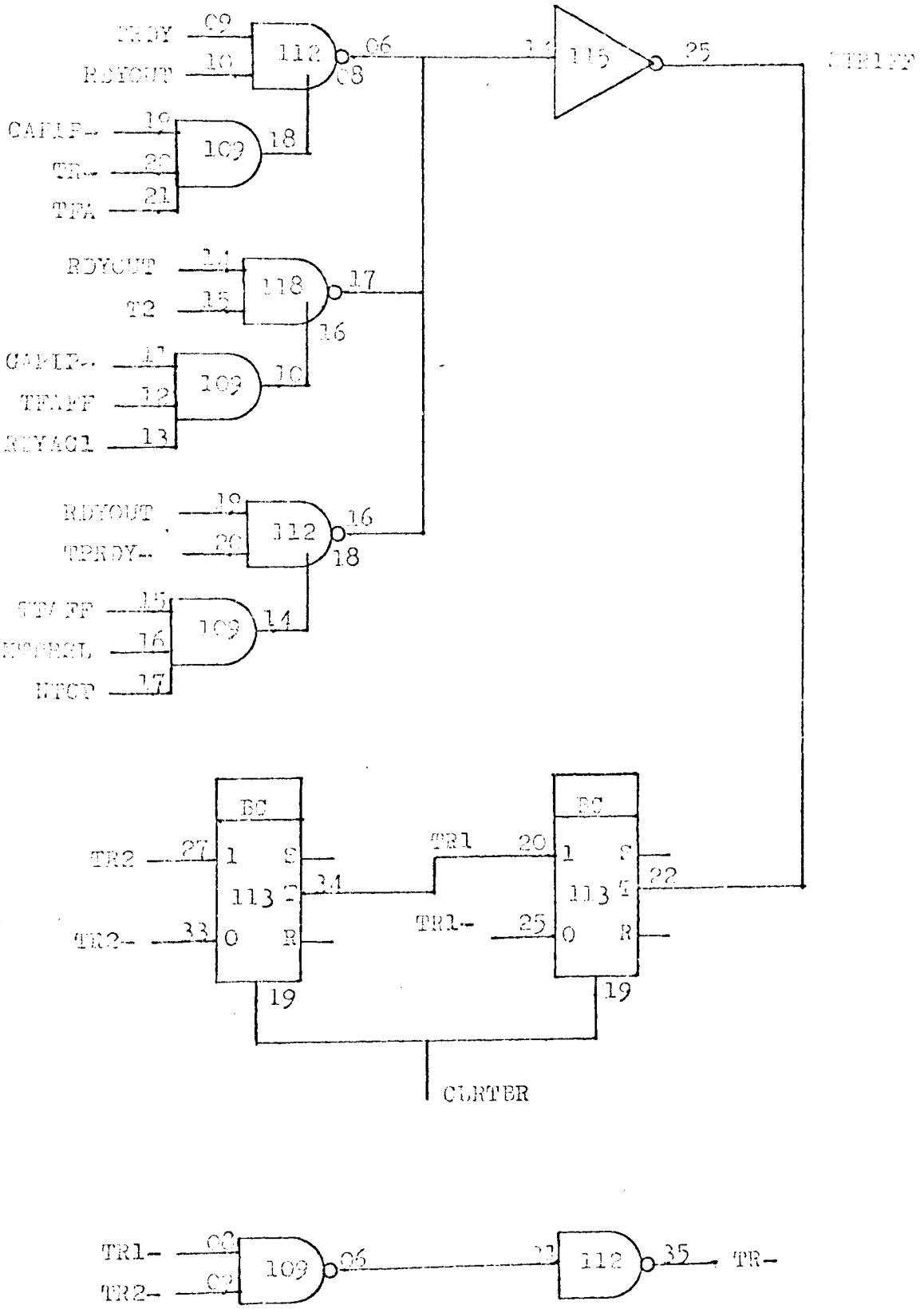

FA
108
107
109
electronic switch
Remote Write Select
XPPJSL
TMRCLR
T6
XTTRST6
Remote Read Select
XTURSL-
TERCLR
105
106
207
209
TPRDY
TMRCLR
TERDY-

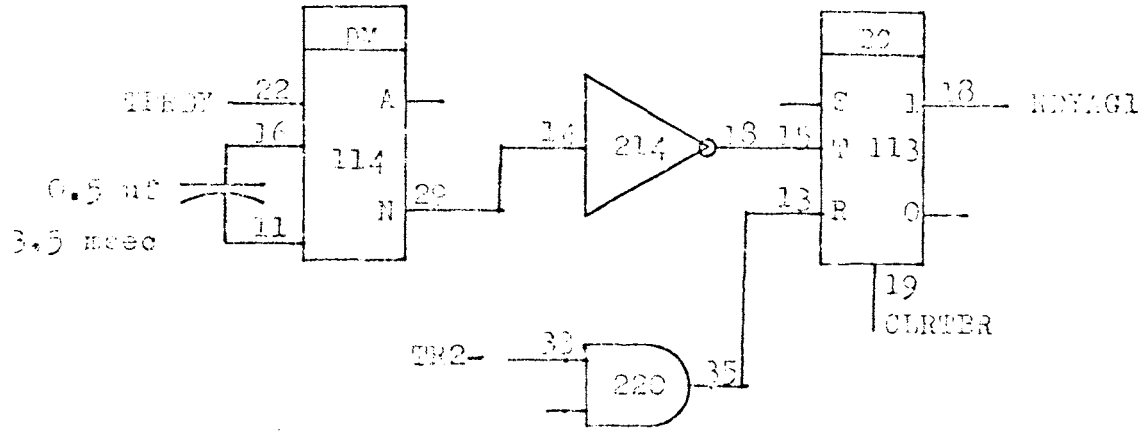

TFAB-
LC1
17
103
12
TFA
09
110
07
TRANSF
14
TTAB-
LC1
19
103
06
TTA
DSTB-
LC1
13
110
16
DST

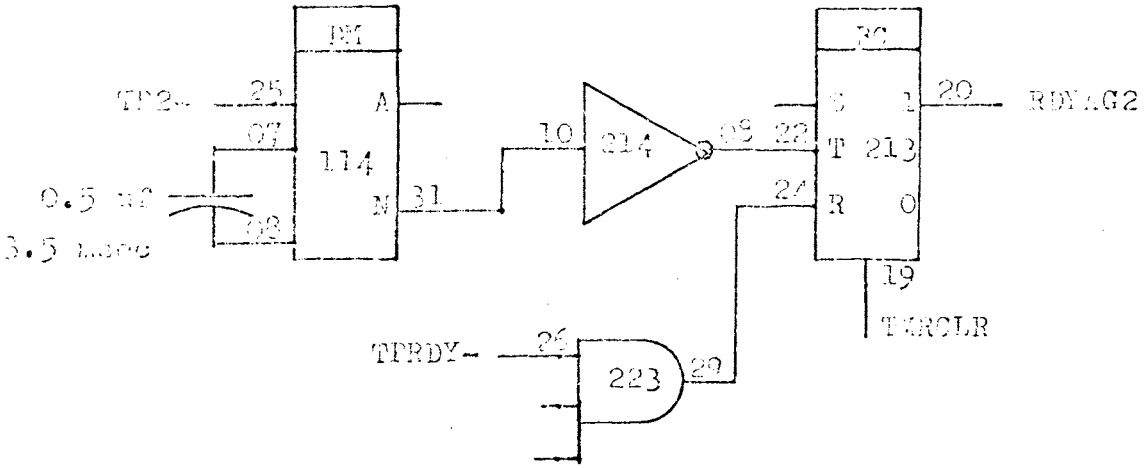

MAGTPW
15
TFA
14
112
11
14
BC
S
1
06
TFAFF
113
R
0
09
TFAFF-
19
CLRTBR

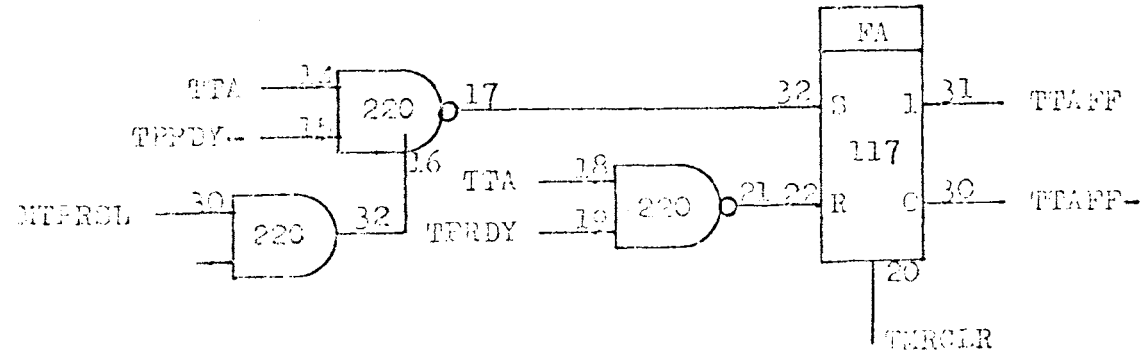

DST
18
TFAFF-
19
118
21
20
22
116
32
35
DSTDTA
TTAFF-
26
MAGTP
27
118
29
30
118
32
TRANSF
17
TPRDY
10
110
12
15
LC2
IDRDYB-
MAGTP
34
GAPIP-
35
106
33

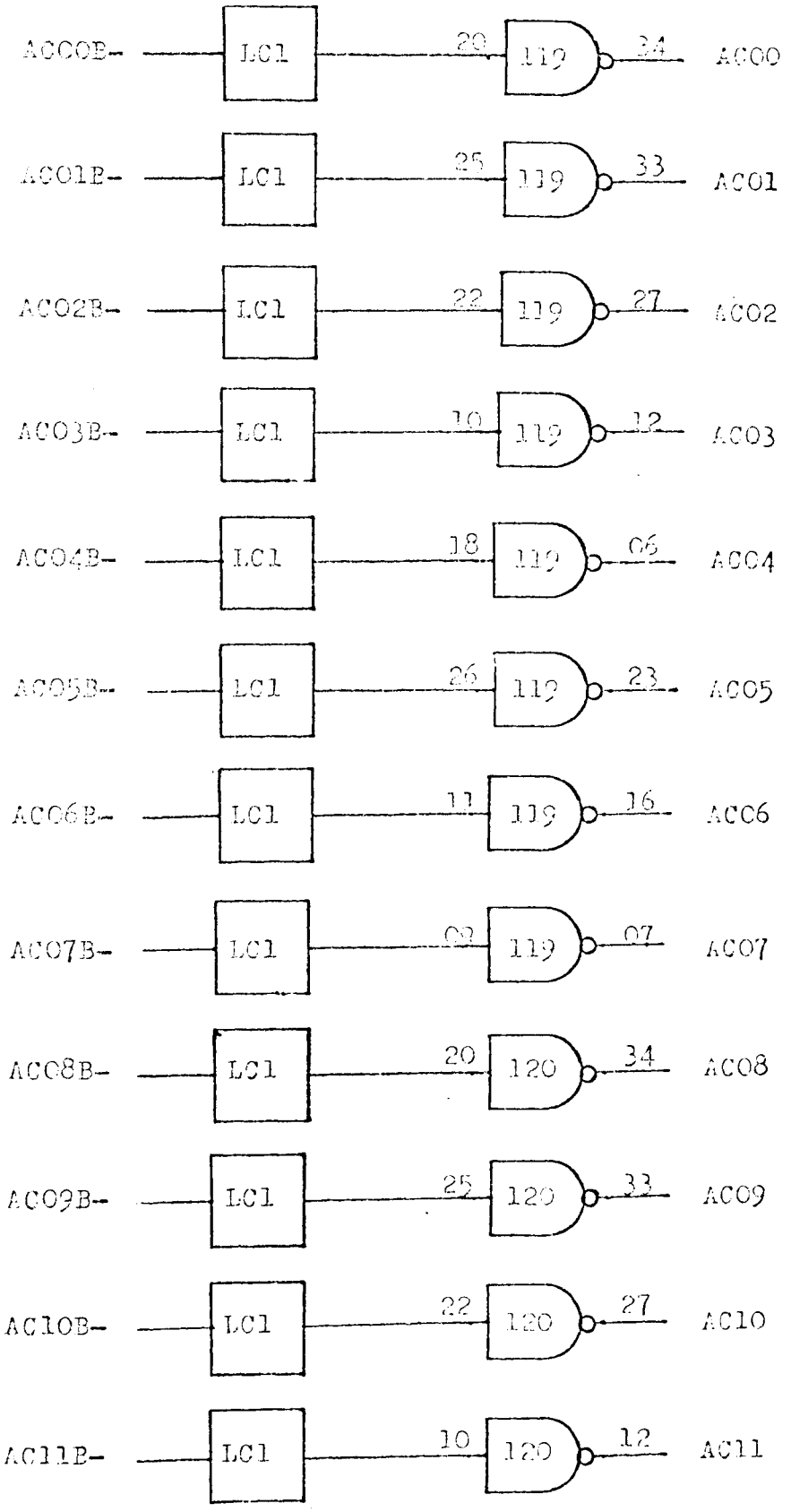

SEL
T2
107
MAGTP
109
TAR
T2
107
MAGTP
109
OTCLEAR
LC1
205
107
111
207
111
RRDYFF
207
RDYOUT
105
MTPWSL
RDYAG2
TO
106
112
SRI
107
TTADT2
105

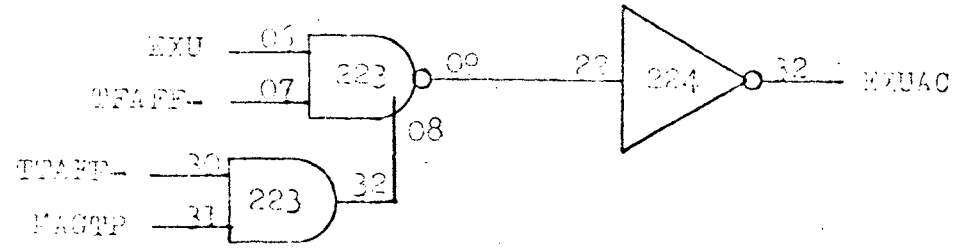

112
109
118
109
112
109
BC
BC
CLRTBR
109
112
TR-

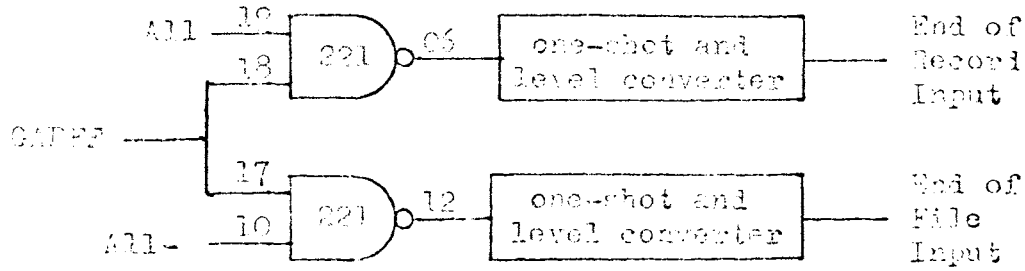

PM
TIRDY
22
16
0.5 mf
3.5 msec
11
114
A
N
29
214
26
18
19
22
S
1
T 113
R
0
13
19
CLRTER
RDYAG1
TM2-
30
220
35

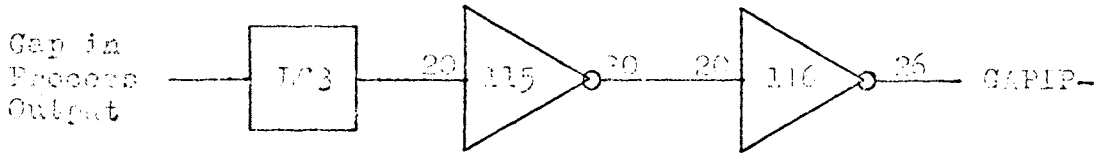

JM
TM2-
25
07
0.5 mf
3.5 msec
08
114
A
N
31
214
10
09
22
RC
S
1
T 213
R
0
24
20
19
RDYAG2
TRRCLR
TPRDY-
26
223
29

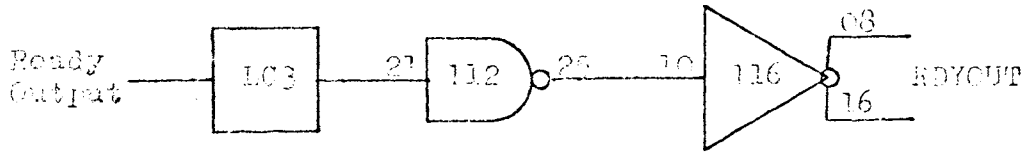

TTA
14
TPPDY-
15
220
17
16
NTFRCL
30
220
32
TTA
18
TPRDY
19
220
21
22
FA
S
1
117
R
0
32
31
30
20
TTAFF
TTAFF-
TRRCLR

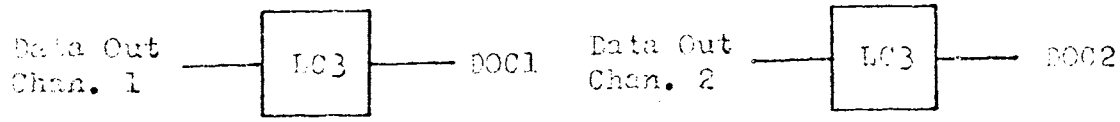

ACC0B-
LC1
20
119
34
ACC0
ACC1B-
LC1
25
119
33
ACC1
ACC2B-
LC1
22
119
27
ACC2
ACC3B-
LC1
10
119
12
ACC3
ACC4B-
LC1
18
119
06
ACC4
ACC5B-
LC1
26
119
23
ACC5
ACC6B-
LC1
11
119
16
ACC6
ACC7B-
LC1
09
119
07
ACC7
ACC8B-
LC1
20
120
34
ACC8
ACC9B-
LC1
25
120
33
ACC9
AC10B-
LC1
22
120
27
AC10
AC11B-
LC1
10
120
12
AC11

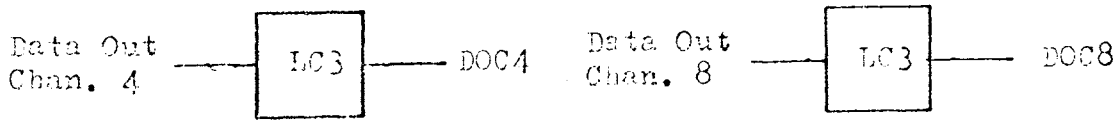

EXU
06
07
223
09
22
224
32
EXUAC
TFAFF-
08
TFAFT-
30
223
32
MAGTP
31

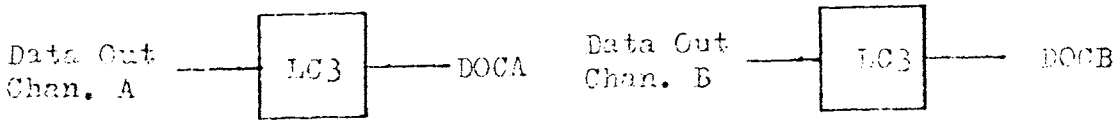

All
19
18
221
06
one-shot and level converter
End of Record Input
CAFFF
17
All-
10
221
12
one-shot and level converter
End of File Input

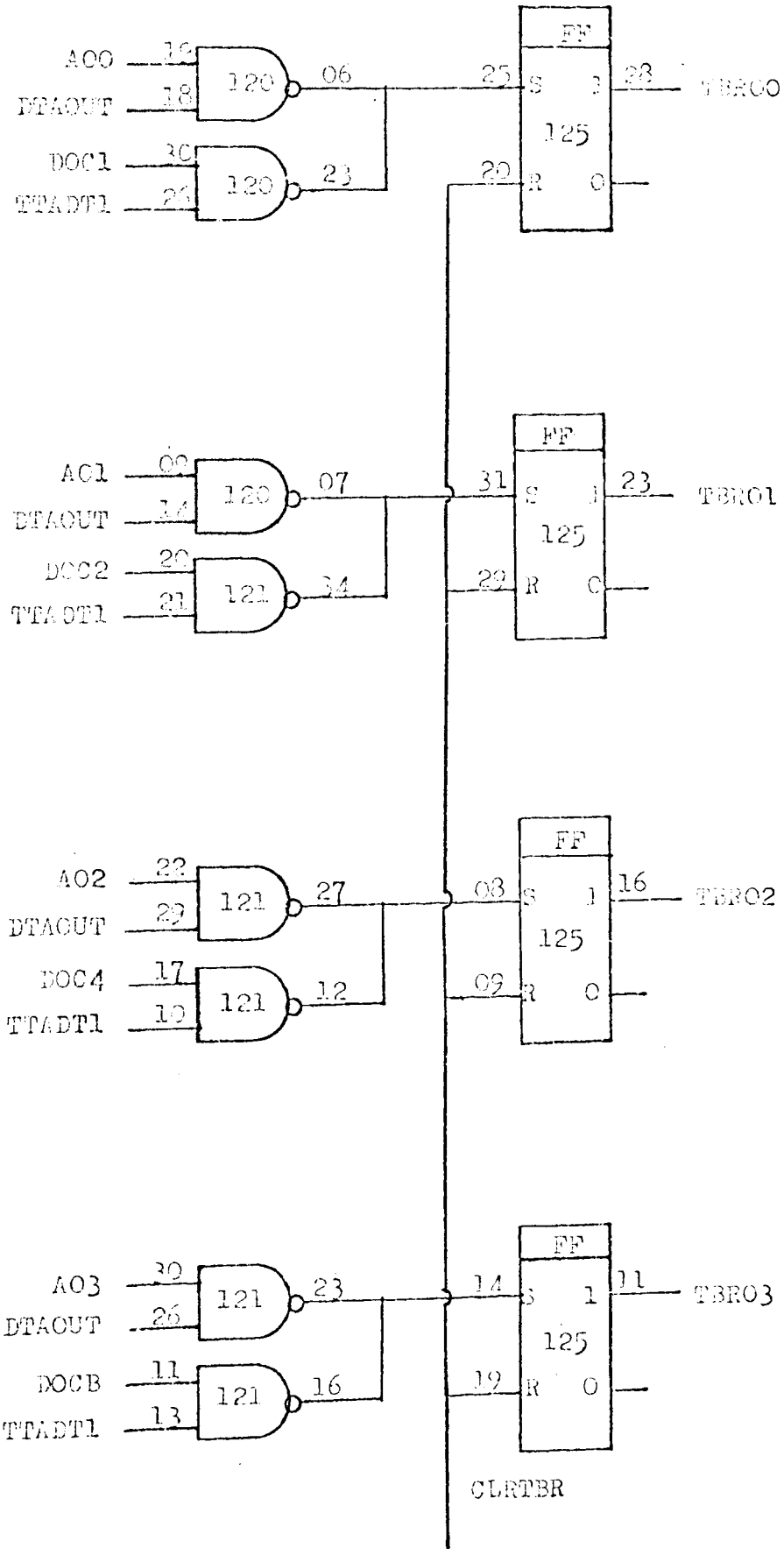

Gap in Process Output
LC3
29
115
30
26
116
25
GAPIP-

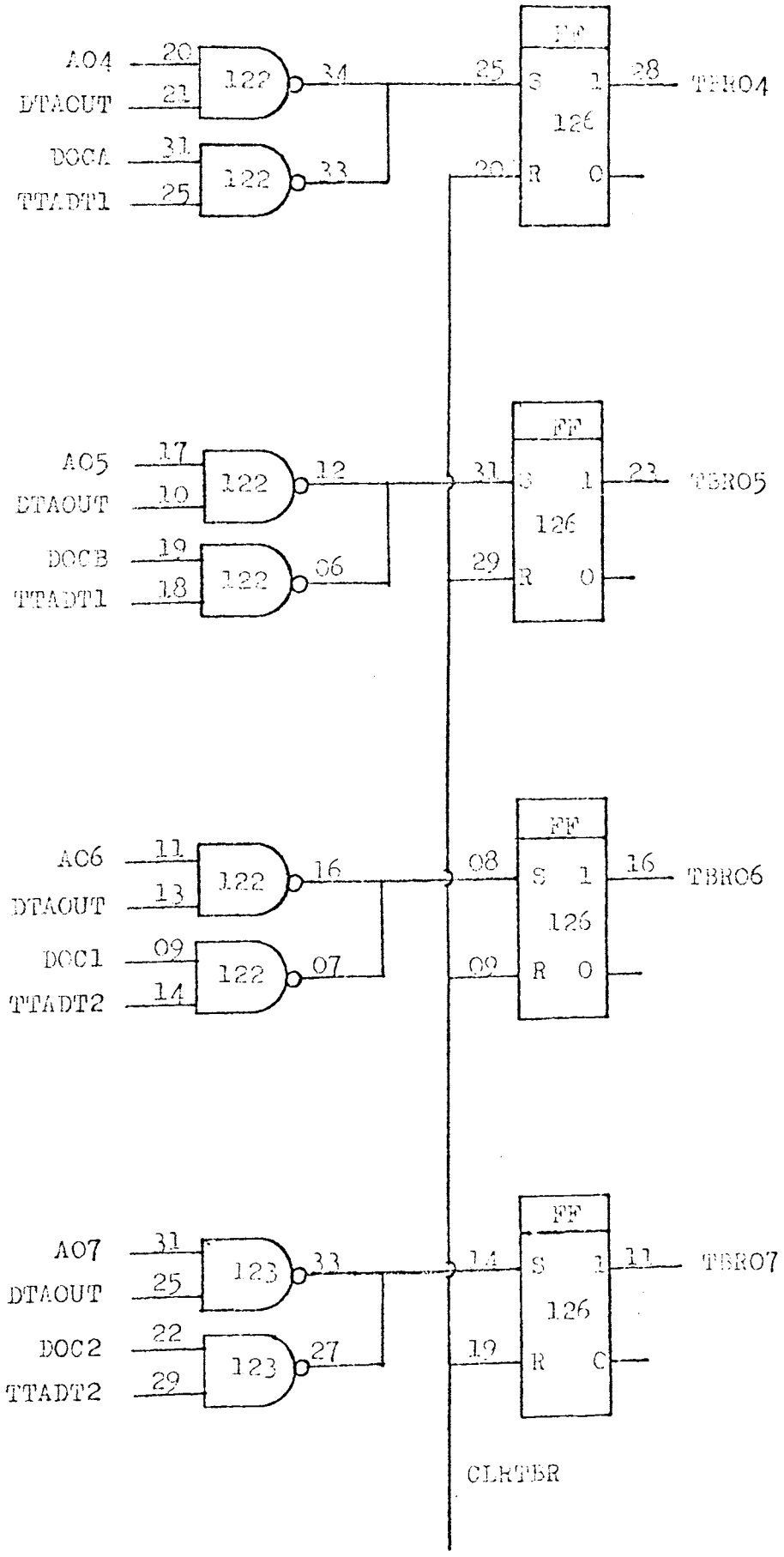

Ready Output
LC3
27
112
25
10
116
08
16
RDYOUT

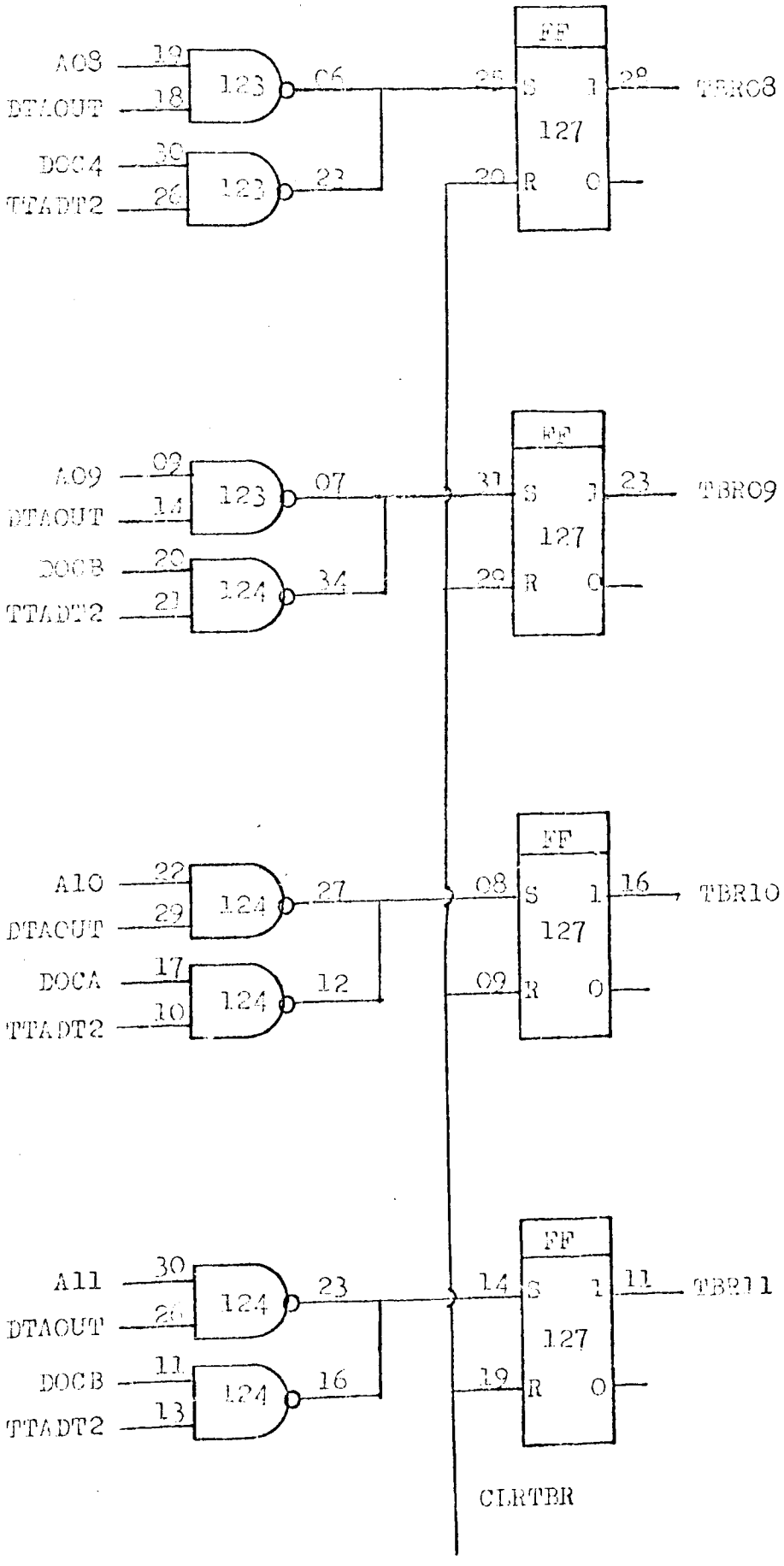

Data Out Chan. 1
LC3
DOC1
Data Out Chan. 2
LC3
DOC2

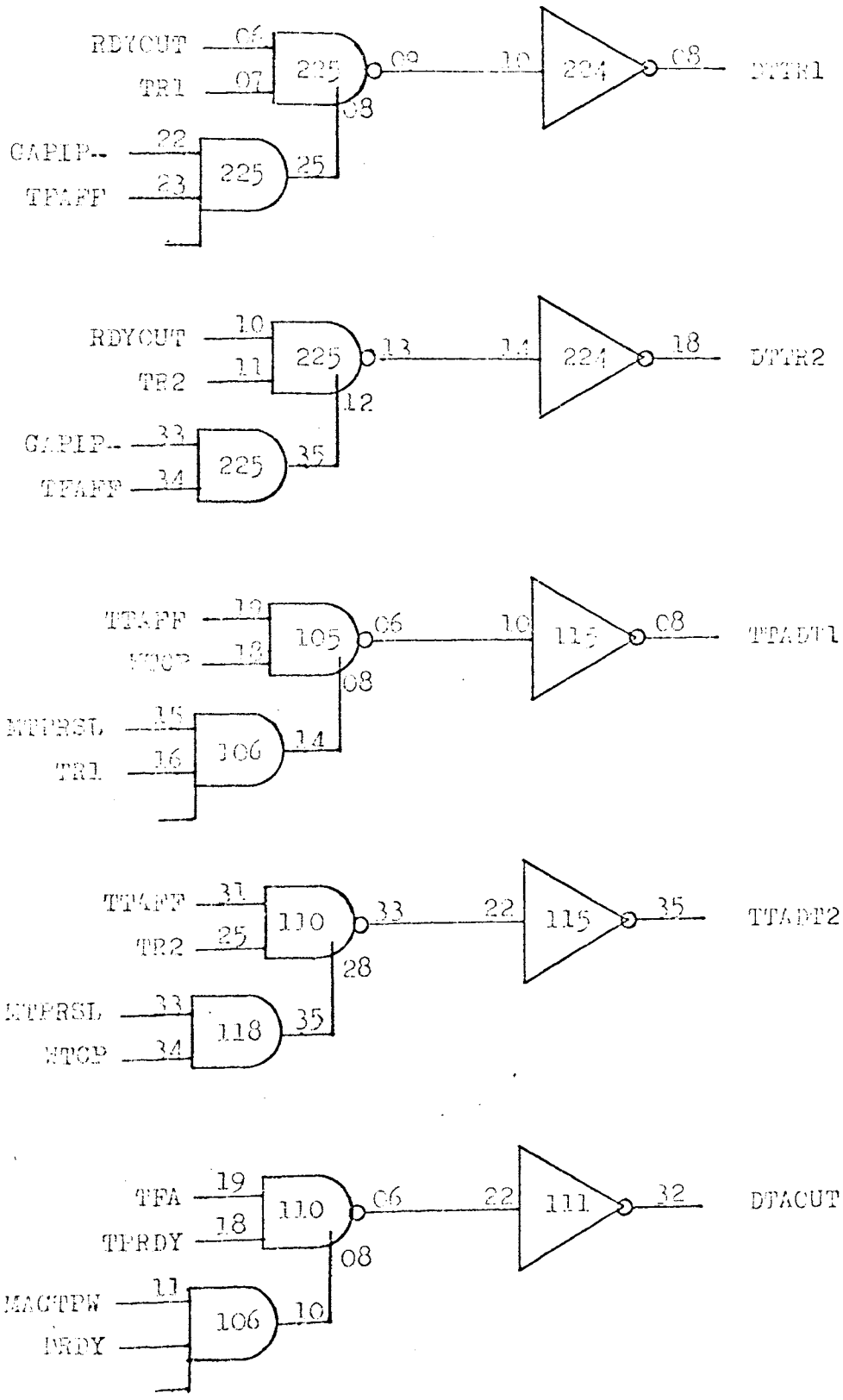

Data Out Chan. 4
LC3
DOC4
Data Out Chan. 8
LC3
DOC8

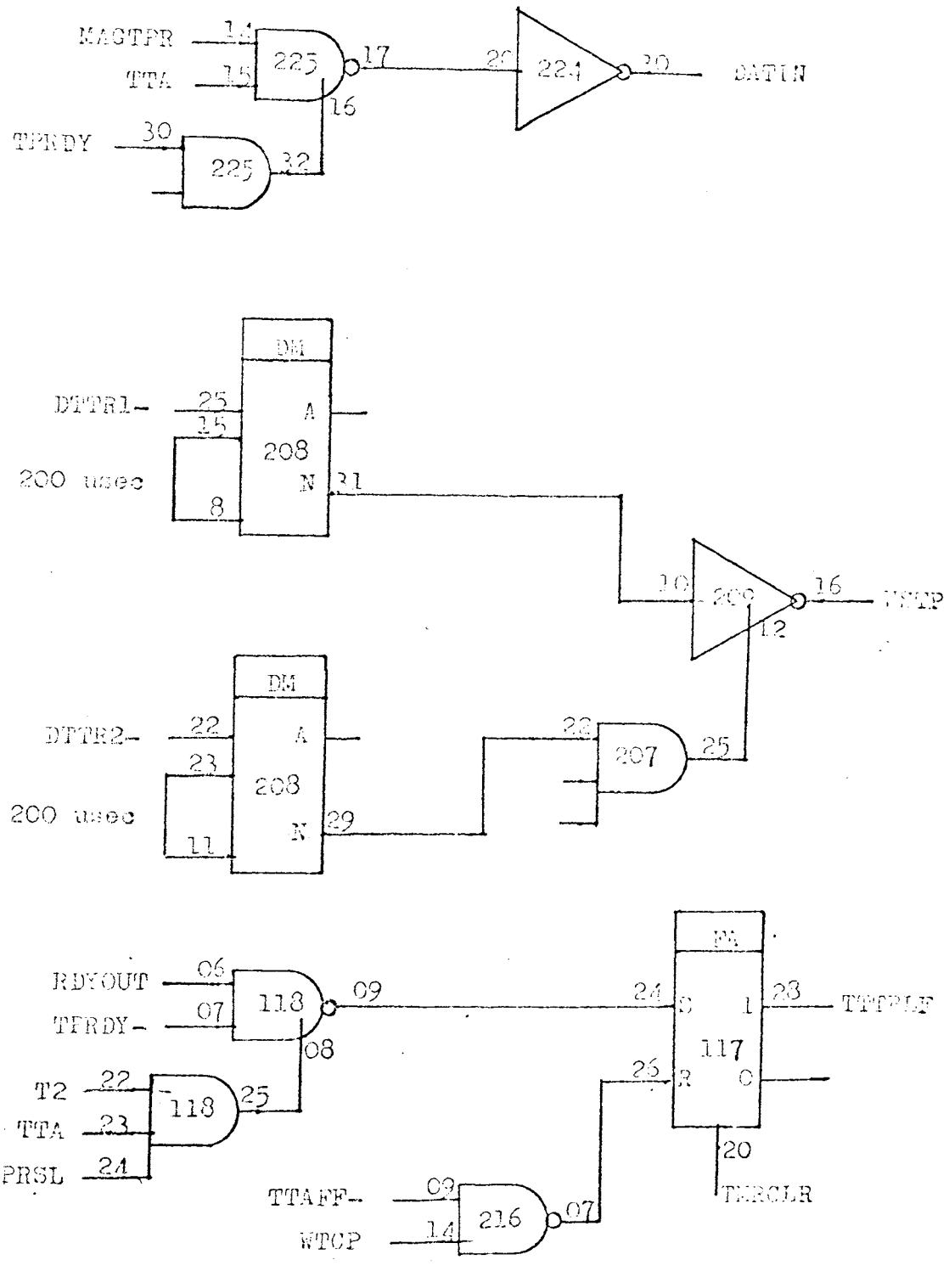

Data Out Chan. A
LC3
DOCA
Data Out Chan. B
LC3
DOCB

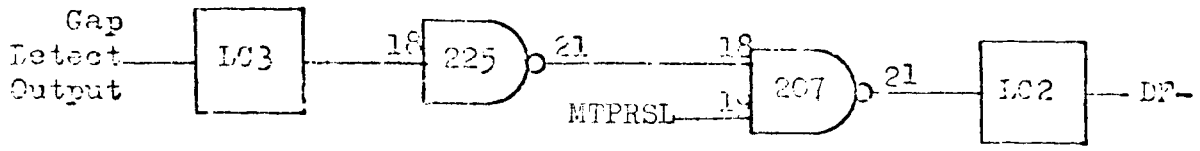

A00
DTAOUT
DOC1
TTADT1
120
120
06
23
FF
125
S
R
1
0
25
20
28
TBRO0
AC1
DTAOUT
DOC2
TTADT1
120
121
07
34
31
29
23
TBRO1
A02
DTAOUT
DOC4
TTADT1
121
121
27
12
08
09
16
TBRO2
A03
DTAOUT
DOCB
TTADT1
121
121
23
16
14
19
11
TBRO3
CLRTBR

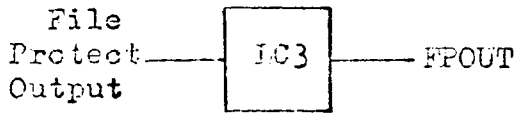

A04
DTAOUT
DOCA
TTADT1
122
122
FF
126
TBR04
A05
DTAOUT
DOCB
TTADT1
122
122
FF
126
TBR05
A06
DTAOUT
DOC1
TTADT2
122
122
FF
126
TBR06
A07
DTAOUT
DOC2
TTADT2
123
123
FF
126
TBR07
CLRTBR

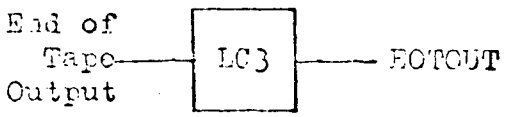

A08
DTAOUT
DOC4
TTADT2
123
124
FF
127
TBR08
A09
DOCB
TBR09
A10
DOCA
TBR10
A11
TBR11
CLRTBR

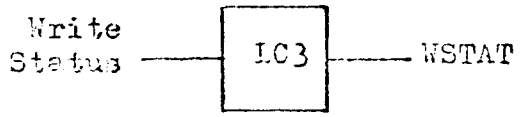

RDYOUT
06
TR1
07
225
09
10
224
08
DTTR1
08
CAPIP--
22
TFAFF
23
225
25
RDYOUT
10
TR2
11
225
13
14
224
18
DTTR2
12
CAPIP--
33
TFAFF
34
225
35
TTAFF
105
06
10
115
08
TTADTT1
08
MTPRSL
15
TR1
16
106
14
TTAFF
31
TR2
25
110
33
22
115
35
TTADT2
28
MTPRSL
33
MTOP
34
118
35
TFA
19
TFRDY
18
110
06
22
111
32
DTACUT
08
MACTPN
11
TRDY
106
10

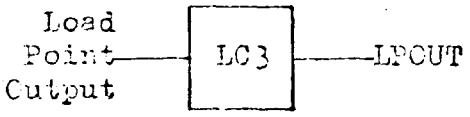

MAGTPR
TTA
TPRDY
225
17
16
30
32
224
DATIN
DM
DTTR1-
25
15
A
208
N
31
8
200 usec
DTTR2-
22
23
11
29
207
25
WSTP
RDYOUT
06
07
118
09
TFRDY-
08
T2
TTA
MTPRSL
24
TTTPLF
117
26
20
TMRCLR
TTAFF-
03
216
WTCP
14
TTAFLF-
11
RLFWD-
13
LC 1
Remote
Load
Forward

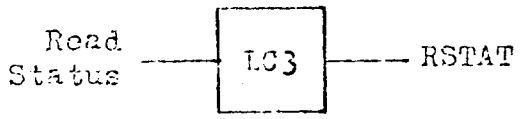

Gap
Detect
Output
LC3
18
225
21
18
MTPRSL
207
21
LC2
DF-

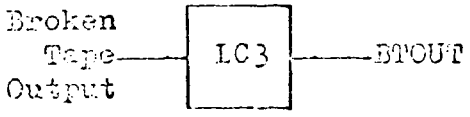

File
Protect
Output
LC3
FPOUT

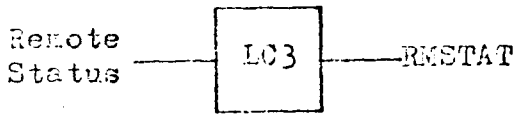

End of
Tape
Output
LC3
EOTOUT

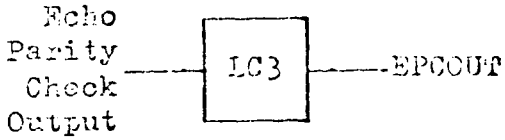

Write
Status
LC3
WSTAT


Load
Point
Output
LC3
LPOUT

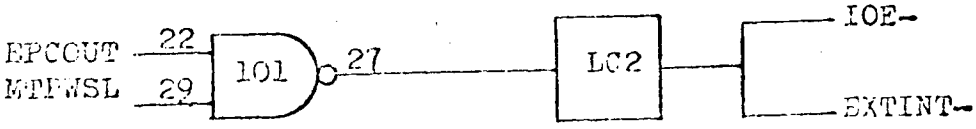

Read
Status
LC3
RSTAT

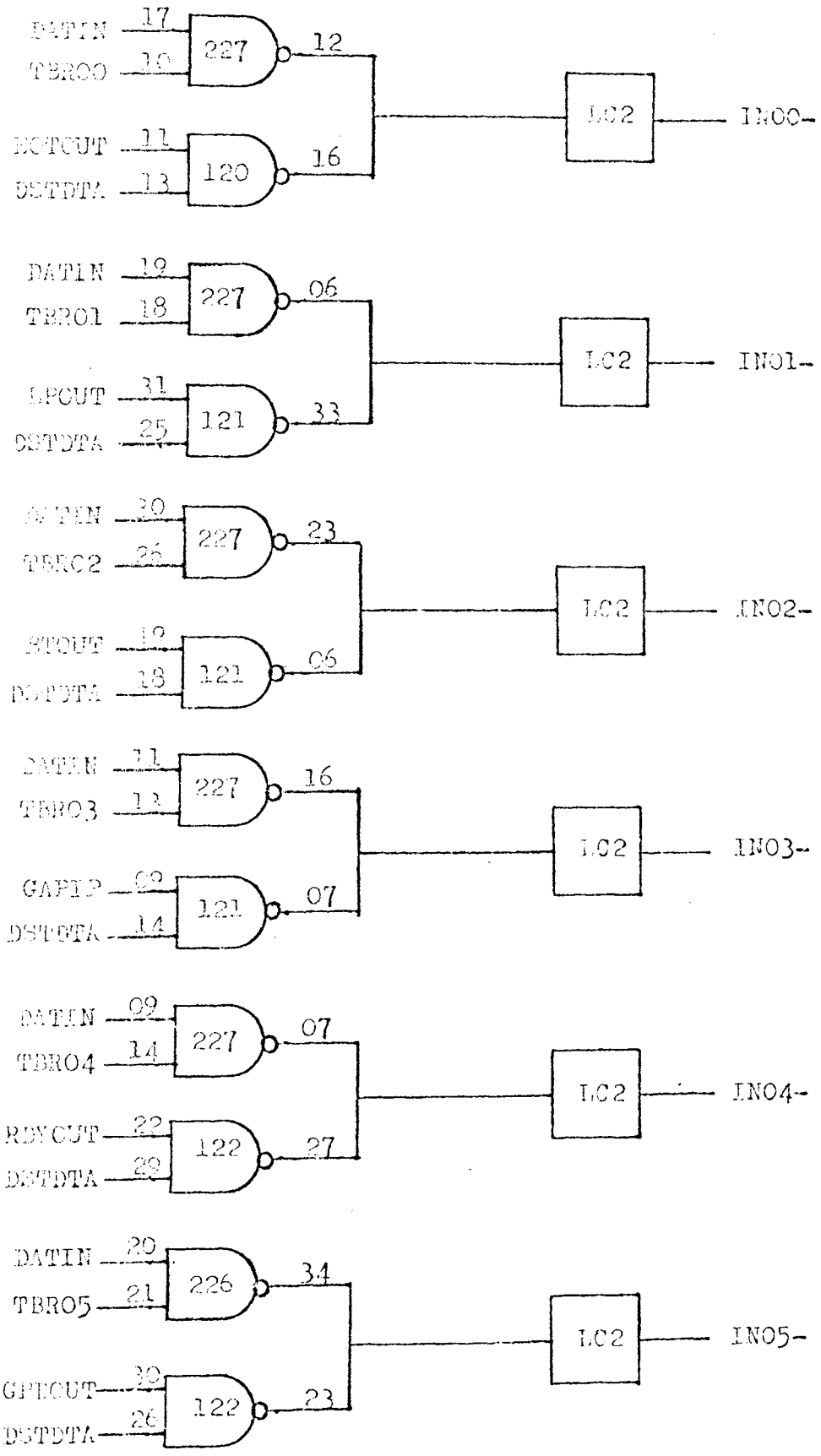

Broken
Tape
Output
LC3
BTOUT

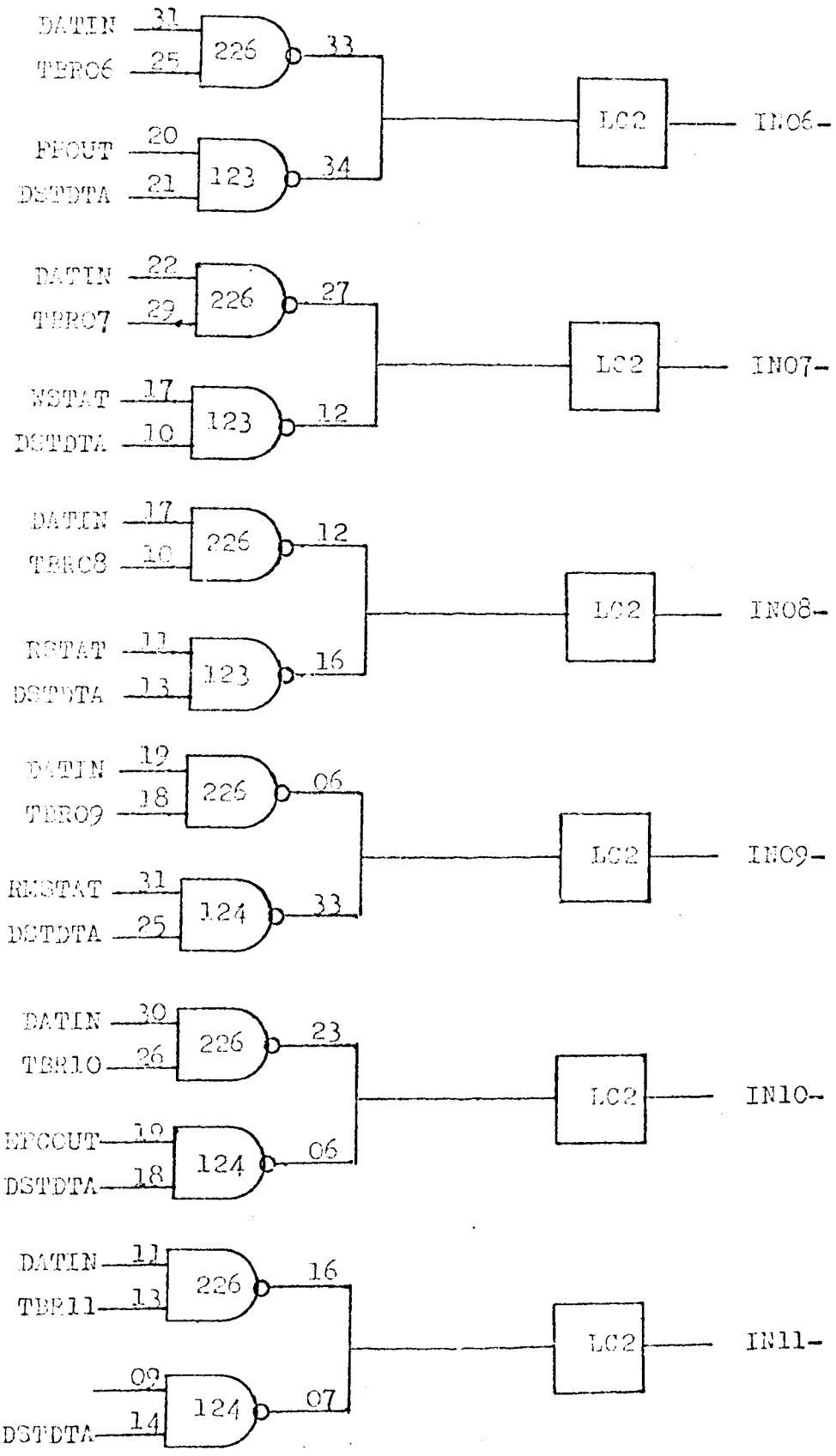

Remote
Status
LC3
RMSTAT

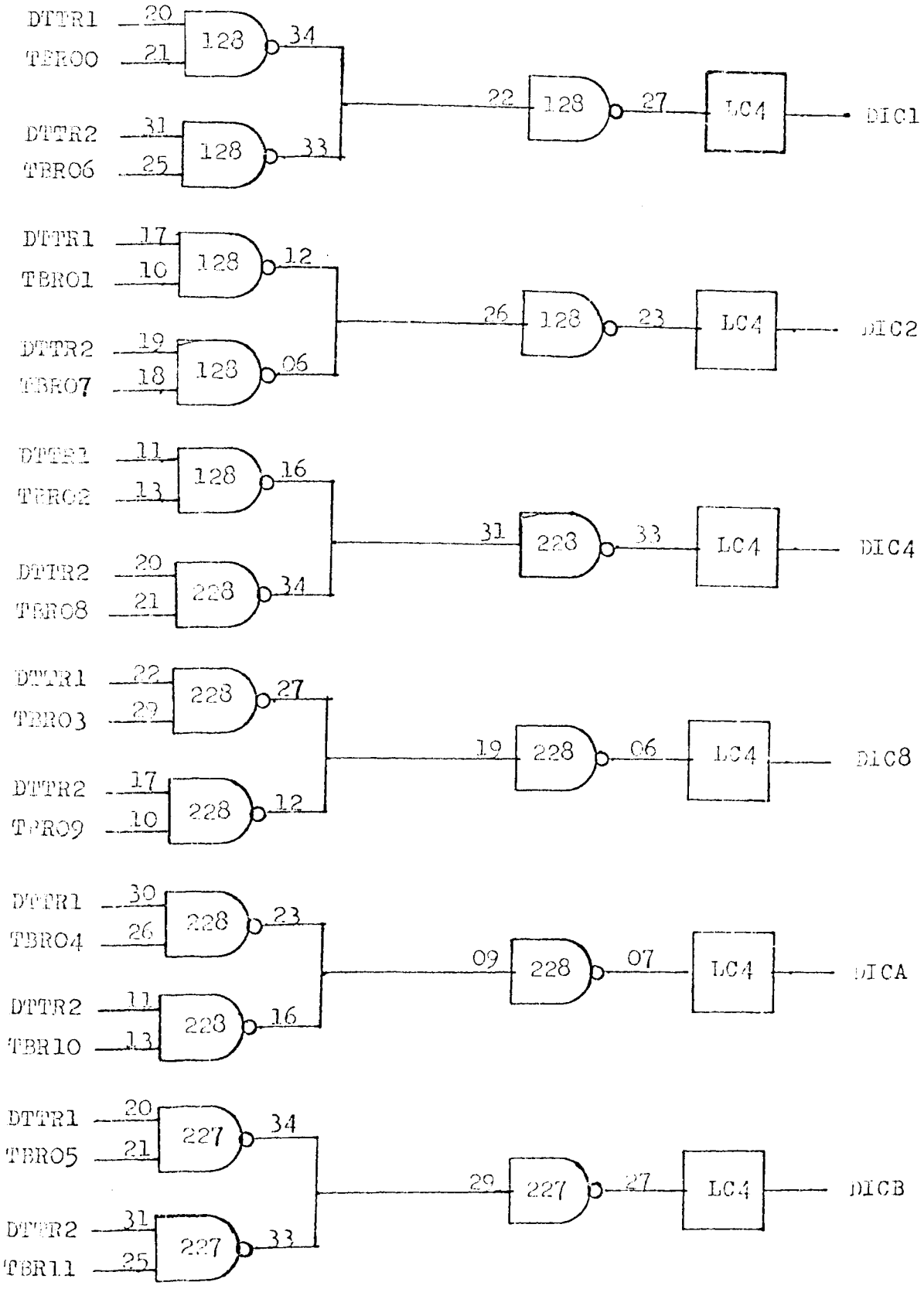

Echo
Parity
Check
Output
LC3
EPCOUT

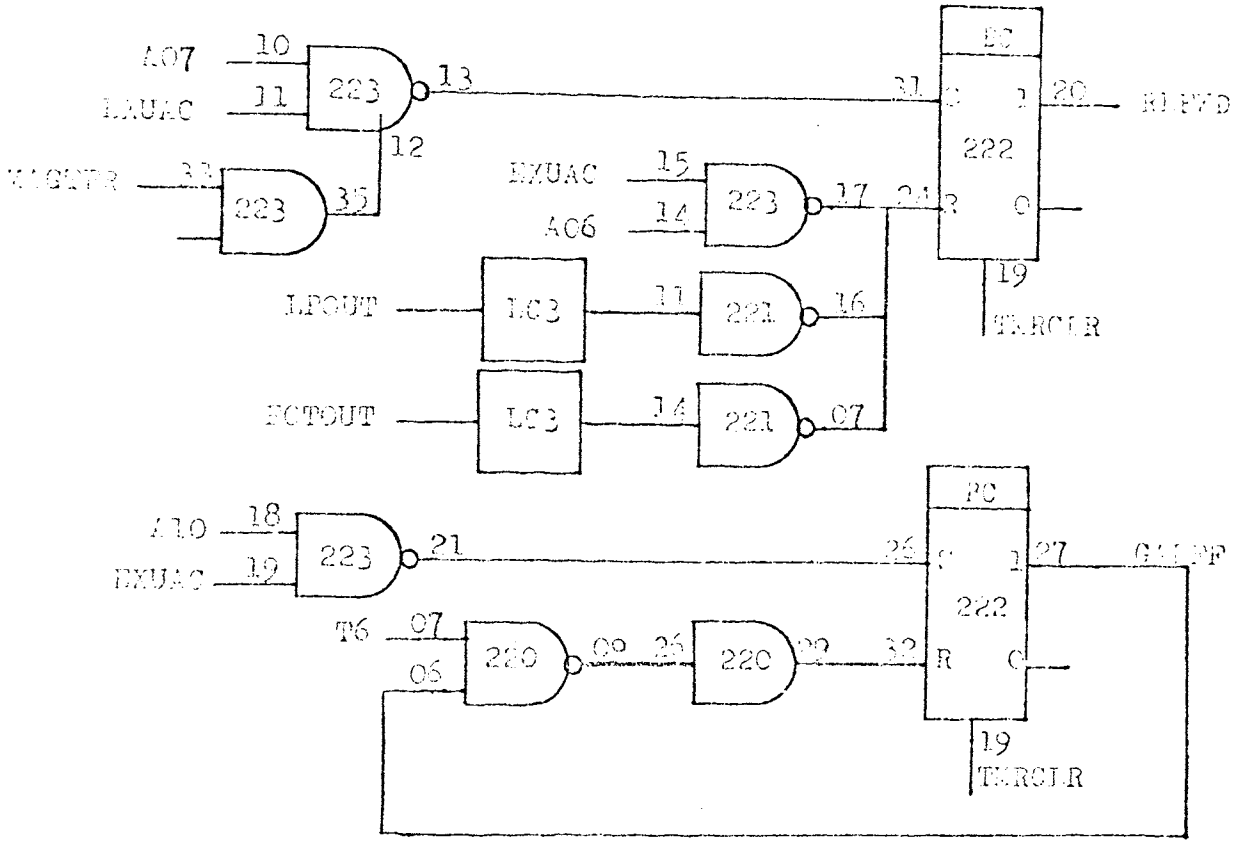

WSTP
one-shot and
level converter
Write-Step Input

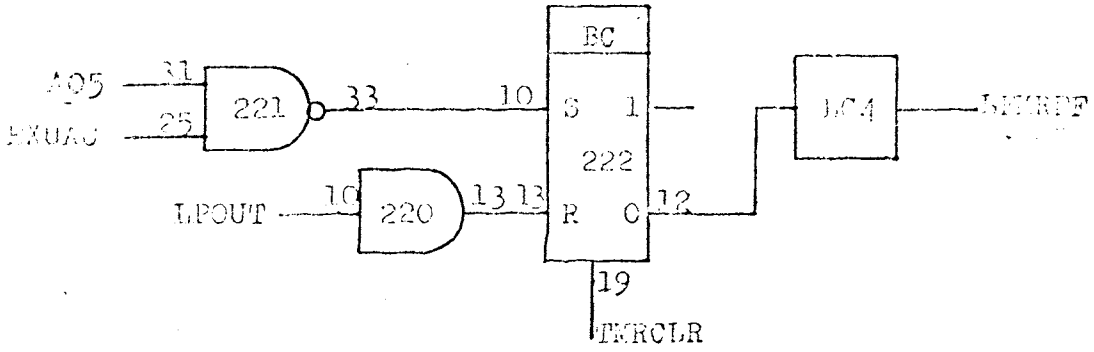

EPCOUT
MTPWSL
22
29
101
27
LC2
IOE-
EXTINT-

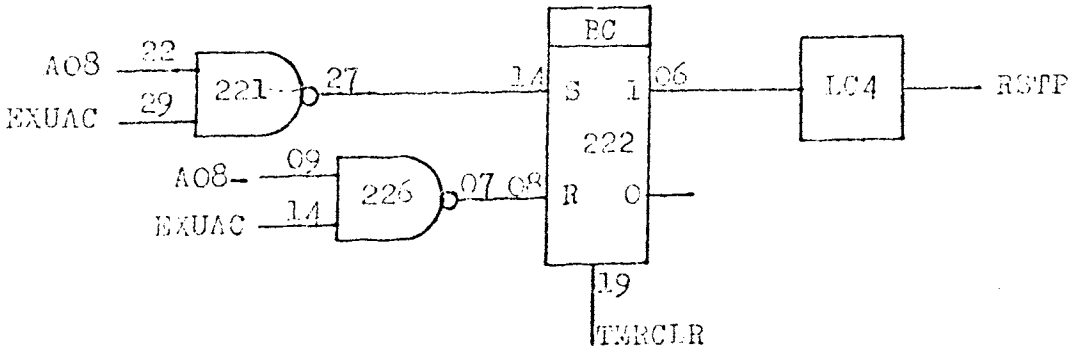

DATIN
17
TBRO0
10
227
12
ECTCUT
11
DSTDTA
13
120
16
LC2
IN00-
DATIN
19
TBRO1
18
227
06
LPCUT
31
DSTDTA
25
121
33
LC2
IN01-
DATIN
30
TBRO2
26
227
23
STOUT
19
DSTDTA
18
121
06
LC2
IN02-
DATIN
11
TBRO3
13
227
16
GAPIP
09
DSTDTA
14
121
07
LC2
IN03-
DATIN
09
TBRO4
14
227
07
RDYOUT
22
DSTDTA
29
122
27
LC2
IN04-
DATIN
20
TBRO5
21
226
34
GPIOUT
30
DSTDTA
26
122
23
LC2
IN05-

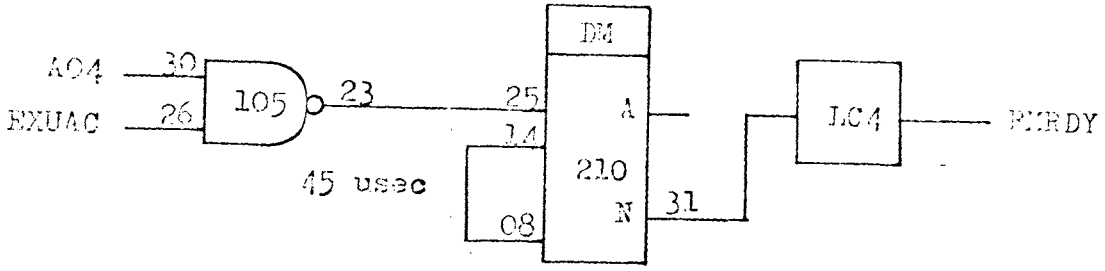

DATIN
TBRO6
226
33
PPOUT
DSTDTA
123
34
LC2
IN06-
DATIN
TBRO7
226
27
WSTAT
DSTDTA
123
12
LC2
IN07-
DATIN
TBRO8
226
12
RSTAT
DSTDTA
123
16
LC2
IN08-
DATIN
TBRO9
226
06
RESTAT
DSTDTA
124
33
LC2
IN09-
DATIN
TBR10
226
23
EPCOUT
DSTDTA
124
06
LC2
IN10-
DATIN
TBR11
226
16
DSTDTA
124
07
LC2
IN11-

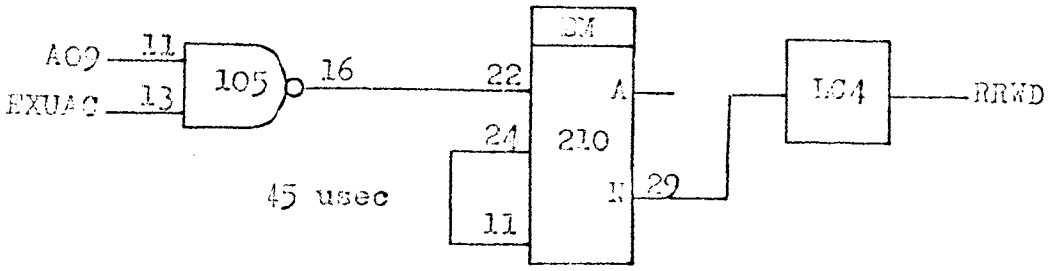

DTTR1
TBRO0
20
21
128
34
DTTR2
TBRO6
31
25
128
33
22
128
27
LC4
DIC1
DTTR1
TBRO1
17
10
128
12
DTTR2
TBRO7
19
18
128
06
26
128
23
LC4
DIC2
DTTR1
TBRO2
11
13
128
16
DTTR2
TBRO8
20
21
228
34
31
228
33
LC4
DIC4
DTTR1
TBRO3
22
29
228
27
DTTR2
TBRO9
17
10
228
12
19
228
06
LC4
DIC8
DTTR1
TBRO4
30
26
228
23
DTTR2
TBR10
11
13
228
16
09
228
07
LC4
DICA
DTTR1
TBRO5
20
21
227
34
DTTR2
TBR11
31
25
227
33
29
227
27
LC4
DICB

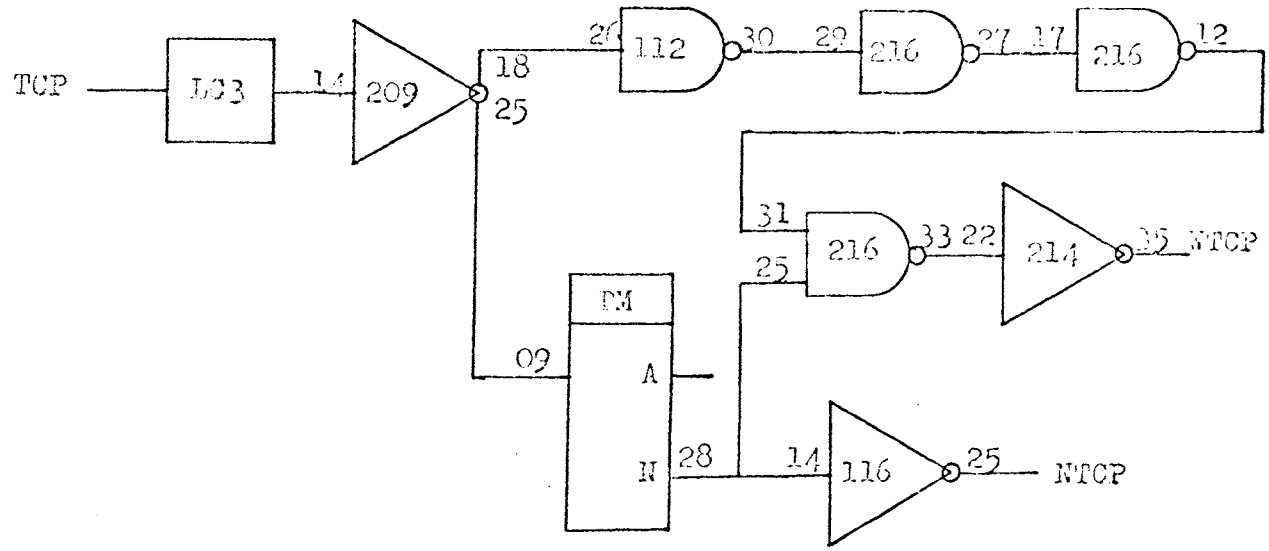

A07
EXUAC
223
223
223
223
223
LC3
LC3
221
221
220
220
222
222
LPOUT
RCTOUT
T6
TMRCLR
TMRCLR

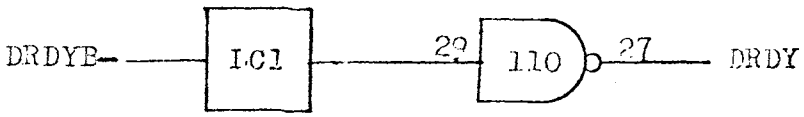

A05
EXUAC
221
LPOUT
220
222
LC4
TMRCLR


A08
EXUAC
221
A08
EXUAC
226
222
LC4
RSTP
TMRCLR


A04
30
EXUAC
26
105
23
25
14
08
45 usec
DM
A
210
N
31
LC4
PIRDY


A09
11
EXUAC
13
105
16
22
24
11
45 usec
DM
A
210
N
29
LC4
RRWD


TCP
LC3
14
209
18
25
26
112
30
29
216
27
17
216
12
31
216
33
22
214
25
NTCP
DM
09
A
N
28
14
116
25
NTCP


DRDYB
LC1
29
110
27
DRDY

Location	Model No.	Description
101	DI-20	NAND Type 2 Pac
102	DC-20	Diode Pac
103	DI-20	NAND Type 2 Pac
104	PA-30	Power Amplifier Pac
105	DI-35	NAND Type 2 Pac
106	DC-35	Diode Pac
107	DI-35	NAND Type 2 Pac
108	FA-35	Gated Flip-Flop Pac
109	DC-20	Diode Pac
110	DI-20	NAND Type 2 Pac
111	PA-35	Power Amplifier Pac
112	DJ-20	Parallel NAND Type 2 Pacs
113	BC-35	Counter Pac
114	DM-35	Delay Multivibrator
115	PA-30	Power Amplifier Pac
116	PA-30	Power Amplifier Pac
117	FA-35	Gated Flip-Flop Pac
118	DN-35	NAND Type 1 Pac
119	DI-20	NAND Type 2 Pac
120	DI-20	NAND Type 2 Pac
121	DI-20	NAND Type 2 Pac
122	DI-20	NAND Type 2 Pac
123	DI-20	NAND Type 2 Pac

Table VIII. Location of S-Pac Cards

Location	Model No.	Description
124	DI-20	NAND Type 2 Pac
125	FF-35	Basic Flip-Flop Pac
126	FF-35	Basic Flip-Flop Pac
127	FF-35	Basic Flip-Flop Pac
128	DI-20	NAND Type 2 Pac
201	PA-30	Power Amplifier Pac
202	PA-30	Power Amplifier Pac
203	PA-30	Power Amplifier Pac
204		
205		
206	PA-30	Power Amplifier Pac
207	DN-35	NAND Type 1 Pac
208	DM-20	Delay Multivibrator
209	PA-30	Power Amplifier Pac
210		
211		
212		
213	BC-35	Counter Pac
214	PA-30	Power Amplifier Pac
215		
216	DI-20	NAND Type 2 Pac
217		
218		

Table VIII. Location of S-Pac Cards (continued)

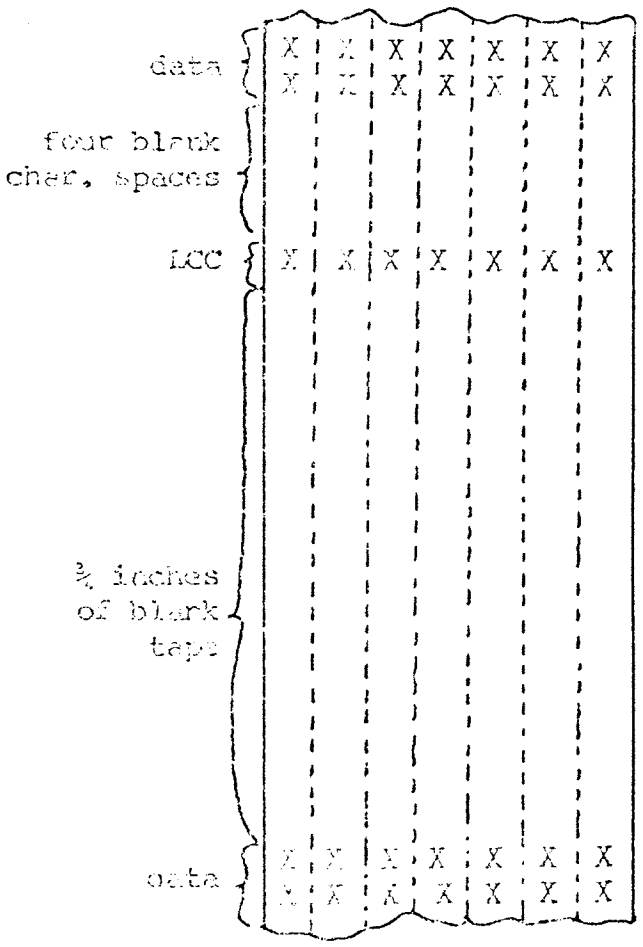
Location	Model No.	Description
219		
220	DN-35	NAND Type 1 Pac
221	DI-20	NAND Type 2 Pac
222	BC-35	Counter Pac
223	DN-20	NAND Type 1 Pac
224	PA-30	Power Amplifier Pac
225	DN-20	NAND Type 1 Pac
226	DI-20	NAND Type 2 Pac
227	DI-20	NAND Type 2 Pac
228	DI-20	NAND Type 2 Pac

Table VIII. Location of S-Pac Cards (continued)

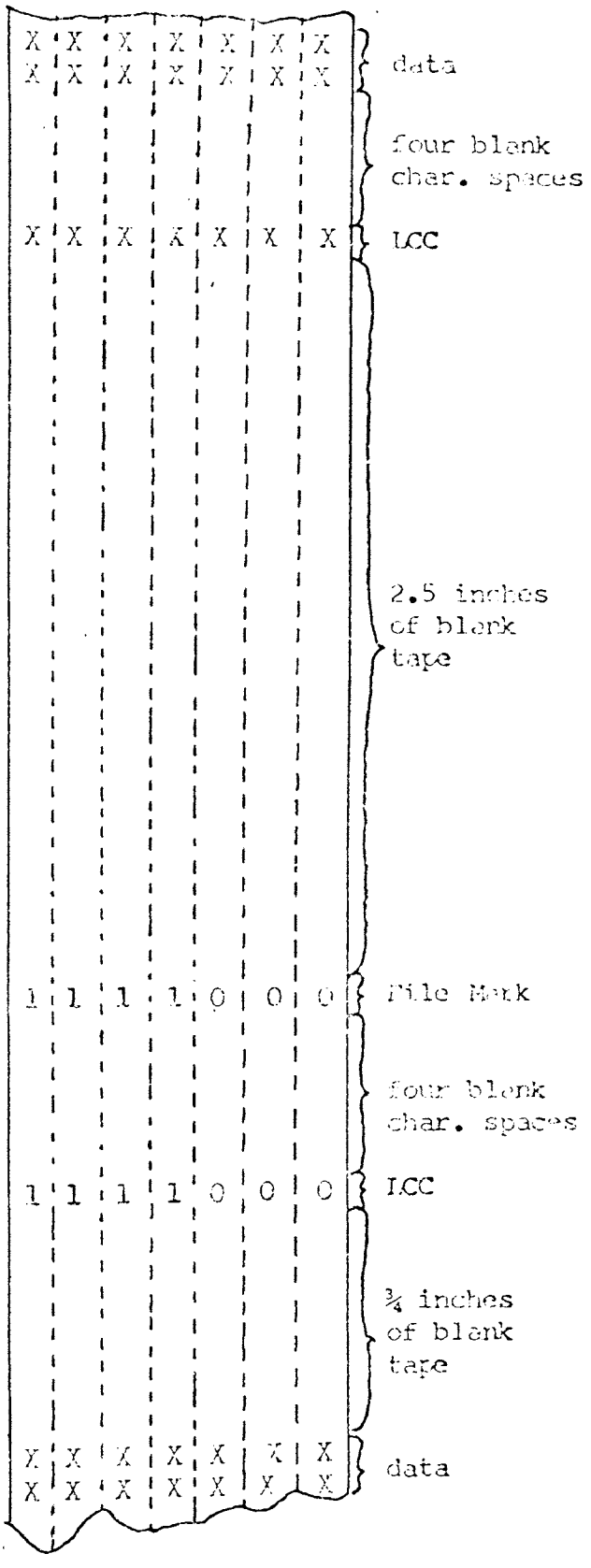
APPENDIX E

Gap Information

At the end of each record, a longitudinal check character (LCC) is recorded in the gap four character spaces after the last data character. This check character is such as to make the total number of bits recorded in any track even for that block. This is another check feature of use in detecting errors. If an End of Record Gap is being produced, 0.75 inches of tape is erased (see Figure 20). If an End of File Gap is being produced 2.5 inches of tape is erased, a file mark (octal 74) is written and followed after four character spaces by its LCC (another octal 74), and then another 0.75 inches of tape is erased.



End of Record Gap



End of File Gap

Figure 20. End of Record and End of File Gaps

APPENDIX F

Example Programs

1. Magnetic Tape Write Routine (all numbers are octal)

Location	Operation Code	Mnemonic		Comments
0000	XXXX	PAR		Starting Address
0001	XXXX	PAR		Ending Address
0002	XXXX	PAR		Header Label
0003	XXXX	PAR		Negative of number of locations
	0734	SEL	34	Select MAGTPW
	6002	LDA	02	Write header label onto tape
	0474	TFA	34	
	2102	JMF	*+2	
	2502	JMB	*-2	
	6000	LDA	00	Calculate negative of number of locations
	6401	SUB	01	
	3403	STA	03	
	6200	LDA*	00	Write program onto tape
	0474	TFA	34	
	2102	JMF	*+2	
	2502	JMB	*-2	
	4000	MIN	00	
	4003	MIN	03	
	2506	JMB	*-6	
	0534	DST	34	Determine when the data transfer has occurred
	2102	JMF	*+2	
	2502	JMB	*-2	

```
0377    SRXC    7,Z
2102    JMF     *+2
2110    JMF     *+10
4120    MIN     *+20
2510    JMB     *-10
```

Compare first two data words with the header label

```
0414    TTA     14
2501    JMB     *-1
0554    SDF     14
2514    JMB     *-14
2504    JMB     *-4
```

Find the beginning of the next gap

```
0414    TTA     14
2102    JMF     *+2
2502    JMB     *-2
3600    STA     *00
4000    MIN     00
4003    MIN     03
2506    JMB     *-6
0654    TMR     14
0000    HLT
XXXX    PAR
```

Load the desired program into the computer at the specified location

VITA

Frederick Harold Keeve, Jr. was born on January 21, 1946, in St. Louis, Missouri and received his primary and secondary education there. He was a co-operative student with Wagner Electric Corporation in St. Louis while working on his Bachelor of Science Degree in Electrical Engineering. He subsequently received this degree in June 1967, from the University of Missouri - Rolla, Missouri.

Since September of 1967, he has been employed by the University of Missouri - Rolla as a Graduate Assistant while concurrently enrolled in the Graduate School of the same institution.